in the current version.

)	8	ESOP-8

PIN CONFIGURATION

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SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range	4.5	85	V
V_{OUT}	Output voltage range	0.8	24	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

$R_{\theta JA}$	Junction to ambient thermal resistance(1)	42	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	45.8	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2A10 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2A10. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=48V, T_J=-40°C~125°C, typical value is tested under 25°C.

V_{IN}	Operating input voltage		4.5	85	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising		4.2	V
	Hysteresis			400	mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		3	μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		100	μA
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		750	mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			500	mΩ

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V_{REF}	Reference voltage of FB		0.792	0.8	0.808	V

V_{EN_H}	Enable high threshold			1.21		V
V_{EN_L}	Enable low threshold			1.05		V
I_{EN_L}	Enable pin pull-up current	EN=1V		1		μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		4		uA
T_{ss}	Internal soft start time			4		ms

F_{RANGE_RT}	Frequency range using RT mode		300		800	kHz
F_{SW}	Switching frequency	R_{RT}=500 kΩ(1%)	420	500	600	kHz
T_{OFF_MIN}	Minimum off-time	V_{IN}=12V		200	260	ns

I_{LIM_P}	LS MOSFET positive current limit	From source to drain		0.8		A
T_{HICCUP}	Hiccup waiting time	Numbers of soft-start cycles		7		cycles
D_{HICCUP}	Hiccup duty cycle			12.5		%

V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising V_{FB}/V_{REF} falling		110 105		% %
T_{SD}	Thermal shutdown threshold	T_J rising Hysteresis		167 35		°C °C

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TYPICAL CHARACTERISTICS

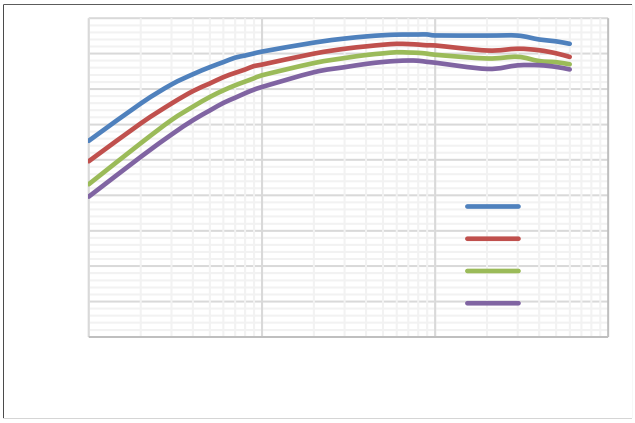

Figure 2. Efficiency vs Load Current (Vout=5V)

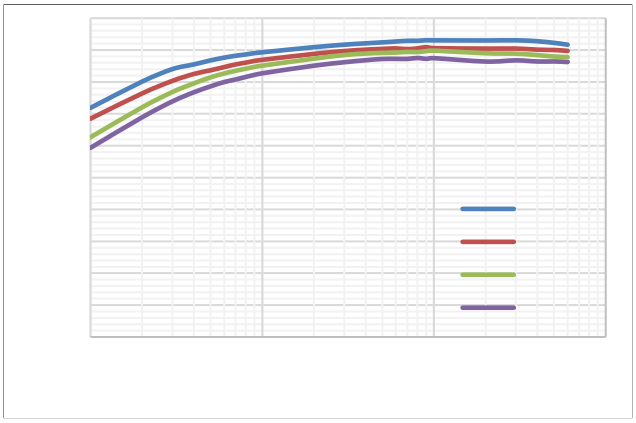

Figure 3. Efficiency vs Load Current (Vout=12V)

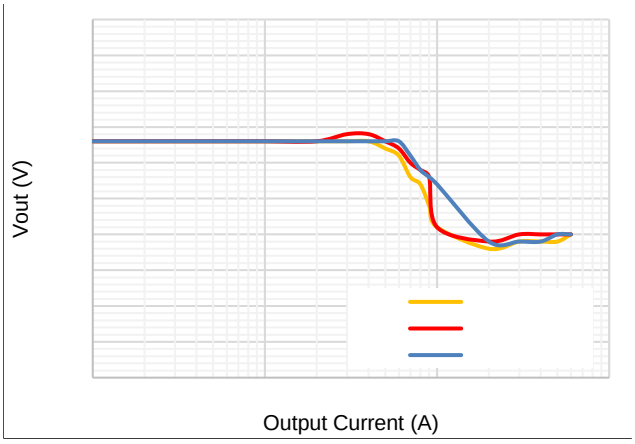

Figure 4. Load Regulation (Vout=12V)

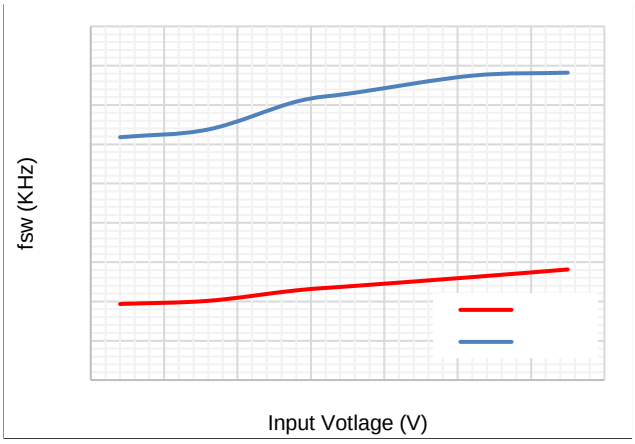

Figure 5 Frequency vs Temperature

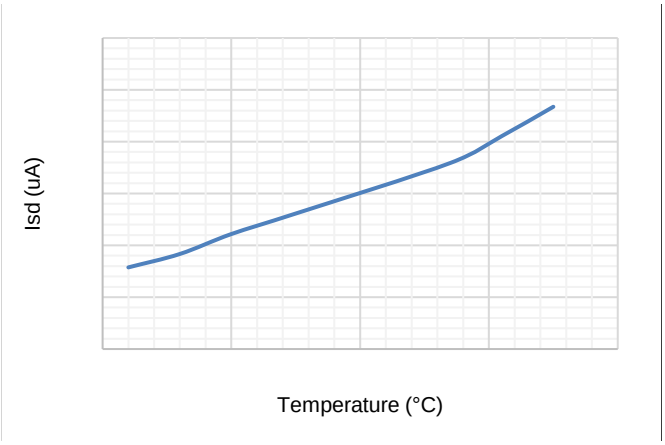

Figure 6. Shut-down Current vs Temperature

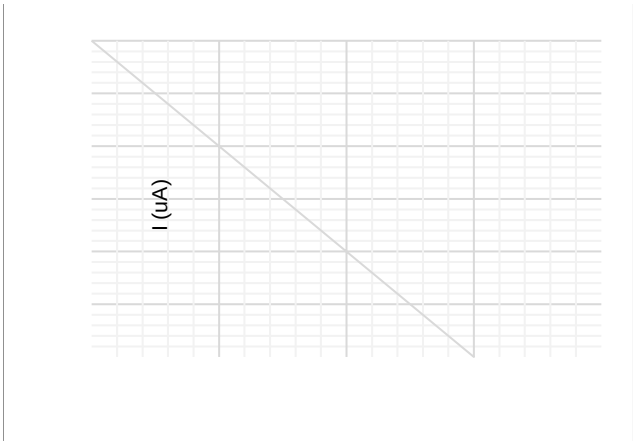

Figure 7. Iq vs Temperature

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OPERATION

The SCT2A10 is a 4.5V-85V input, 0.6A output, internal-compensated synchronous buck converter with built-in 750mΩ Rdson high-side and 500mΩ Rdson low-side power MOSFETs

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7 5 (1)

8 (2)

Where

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1uA
I_2=3uA
V_{ENR}=1.21V
V_{EMF}=1.05V

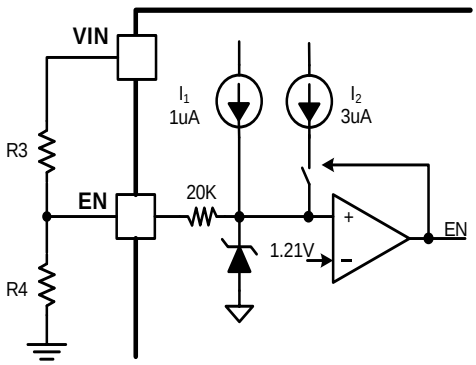

Figure 9. System UVLO by enable divide

The SCT2A10 regulates the internal reference voltage at 0.8V with 1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

5 (3)

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

The SCT2A10 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 4ms. If the EN pin is pulled below 1.05V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

The switching frequency of the SCT2A10 is set by placing a resistor between RT pin and the ground.

In resistor setting frequency mode, a resistor placed between RT pin to the ground sets the switching frequency over a wide range from 300KHz to 800KHz. RT pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot in Figure 10. to determine the resistance for a switching frequency needed.

8

Where,

fsw is switching clock frequency

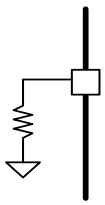

Figure 10. Setting Frequency

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An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The inductor current is monitored during low-side MOSFET Q2 on. The SCT2A10 implements over current protection with cycle-by-cycle limiting low-side MOSFET valley current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

The SCT2A10 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

The SCT2A10 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 167C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 132C, the device restarts with internal soft start phase.

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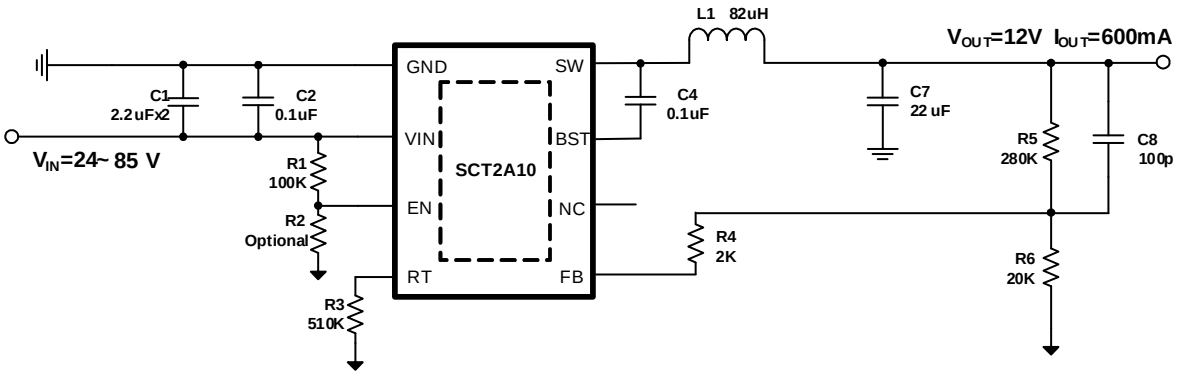
APPLICATION INFORMATION



Input Voltage	48V Normal 24V to 85V
Output Voltage	12V
Maximum Output Current	600mA
Switching Frequency	500 KHz
Output voltage ripple (peak to peak)	50mV
Transient Response 60mA to 540mA load step	ΔVout = 400mV

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The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use equation 5 to calculate R5.

—— 5 (5)

where:

- V_{REF} is the feedback reference voltage, typical 0.8V

An external voltage divider network of R_1 from the input to EN pin

Table 1. R_5, R_6Value for Common Output Voltage (Room Temperature)

3.3 V	63.5 KΩ	20 KΩ
5 V	105 KΩ	20 KΩ
12 V	280 KΩ	20 KΩ
24 V	580 KΩ	20 KΩ

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-4 %

- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 9 to calculate the inductance value.

5

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The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor

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Vin=48V, Vout=12V, unless otherwise noted

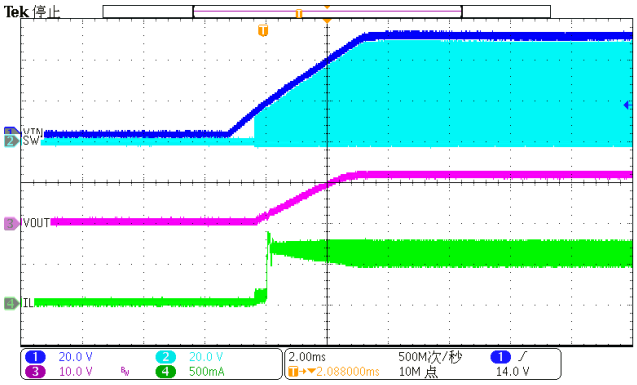

Figure 12. Power up

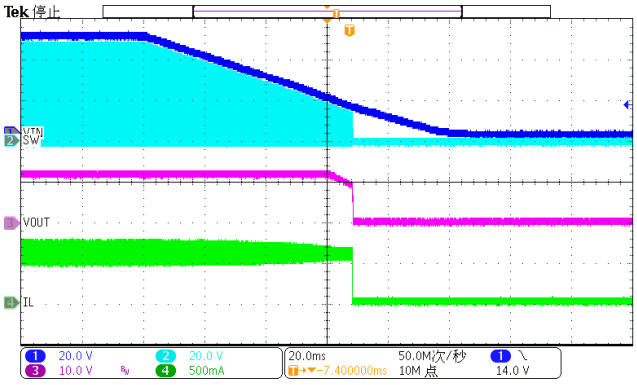

Figure 13. Power down

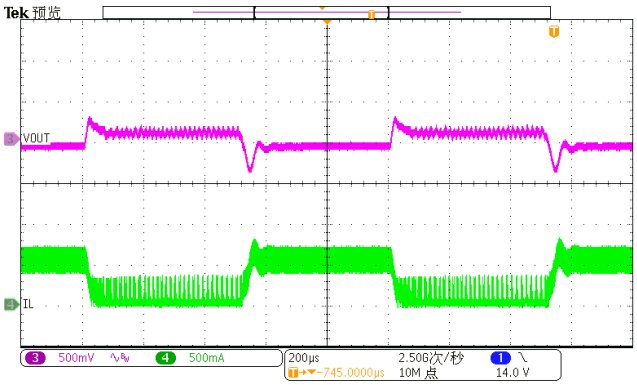

Figure 14.Load Transient (0.06A-0.54A, 0.25A/us)

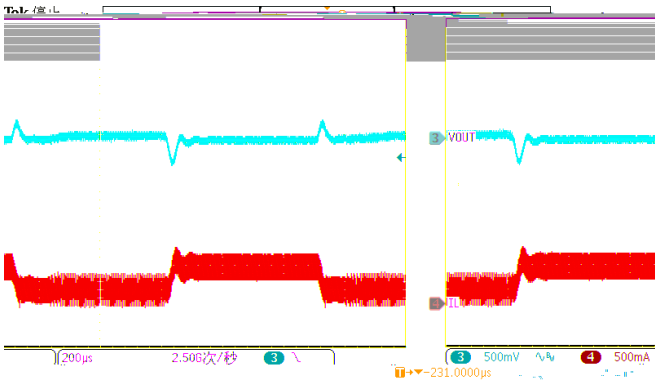

Figure 15. Load Transient (0.15A-0.45A, 0.25A/us)

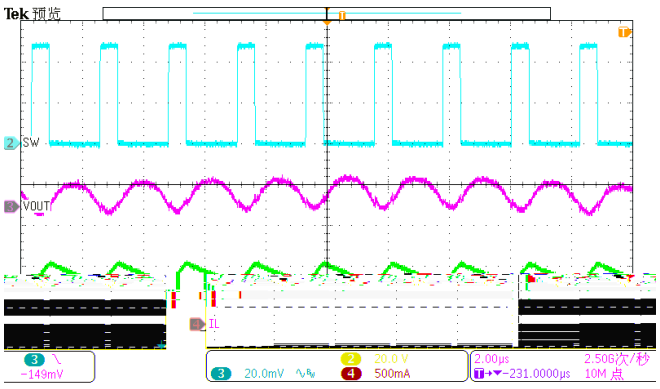

Figure 16. SW and Vout Ripple

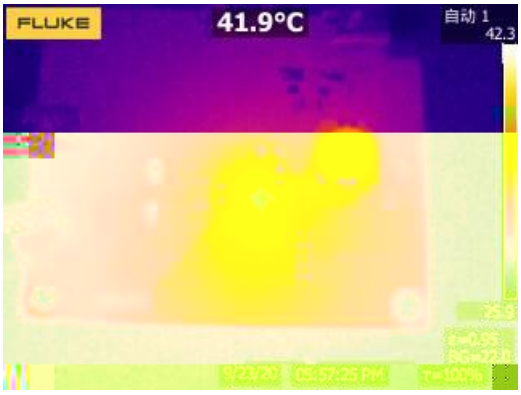

Figure 17. Thermal, 48VIN, 12Vout, 0.6A

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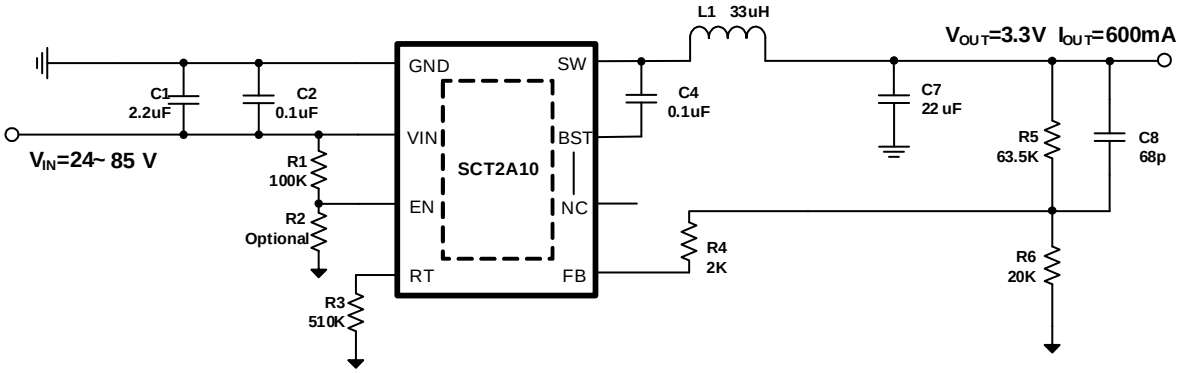

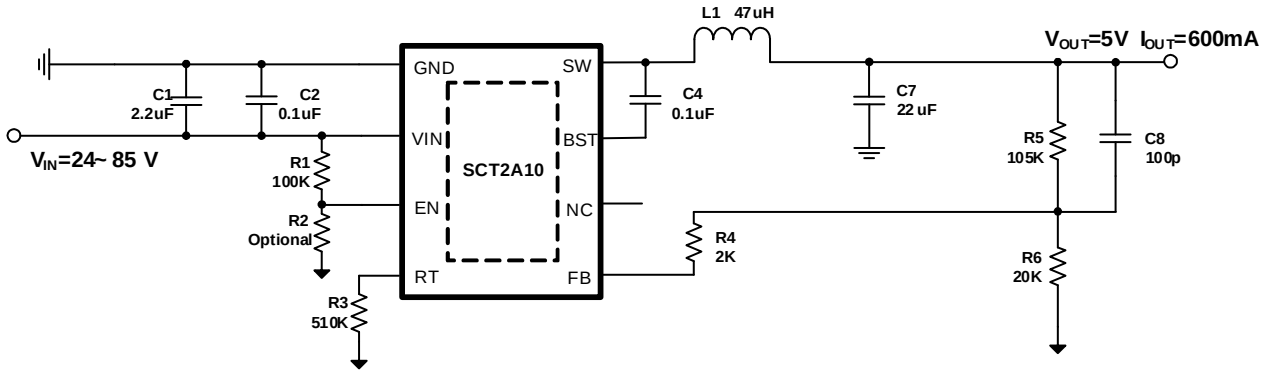

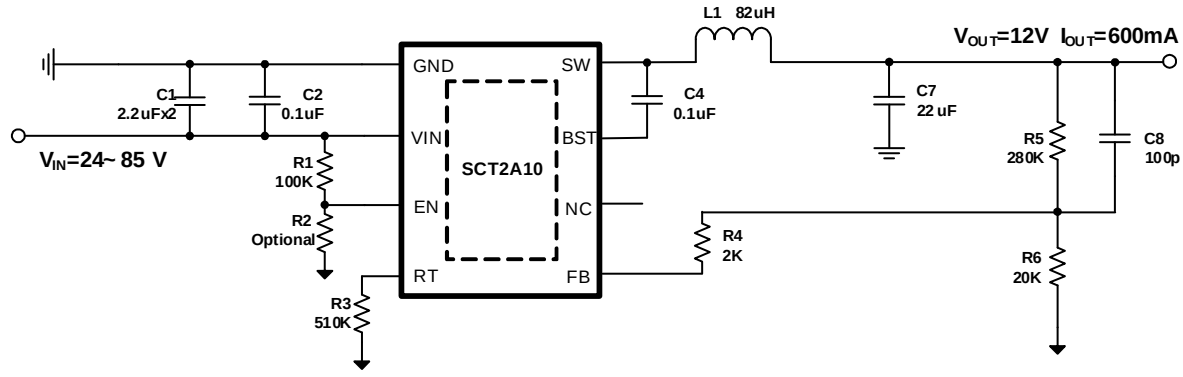

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Proper PCB layout is a critical for SCT2A10's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

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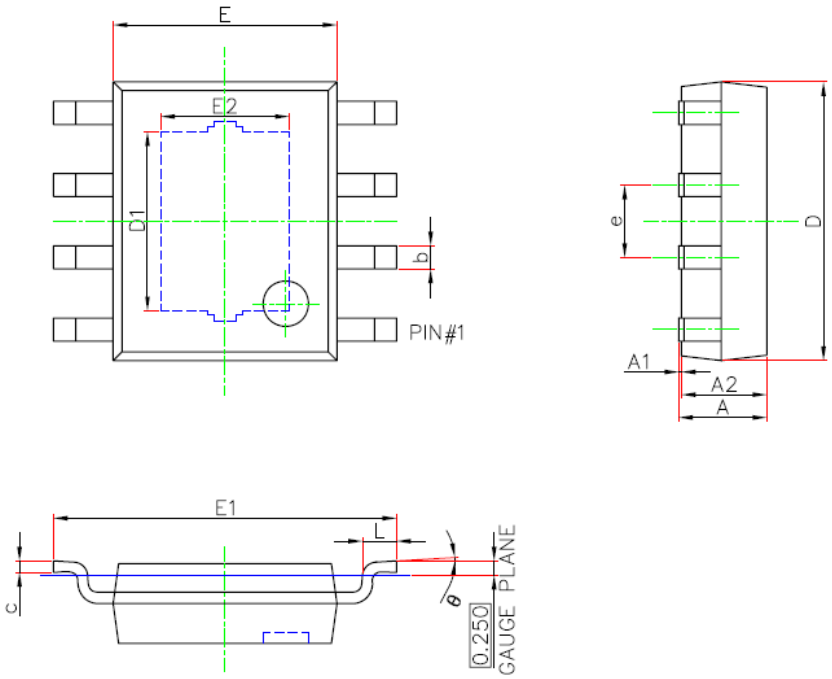
PACKAGE INFORMATION



ESOP8/PP(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
	0°	8°	0°	8°

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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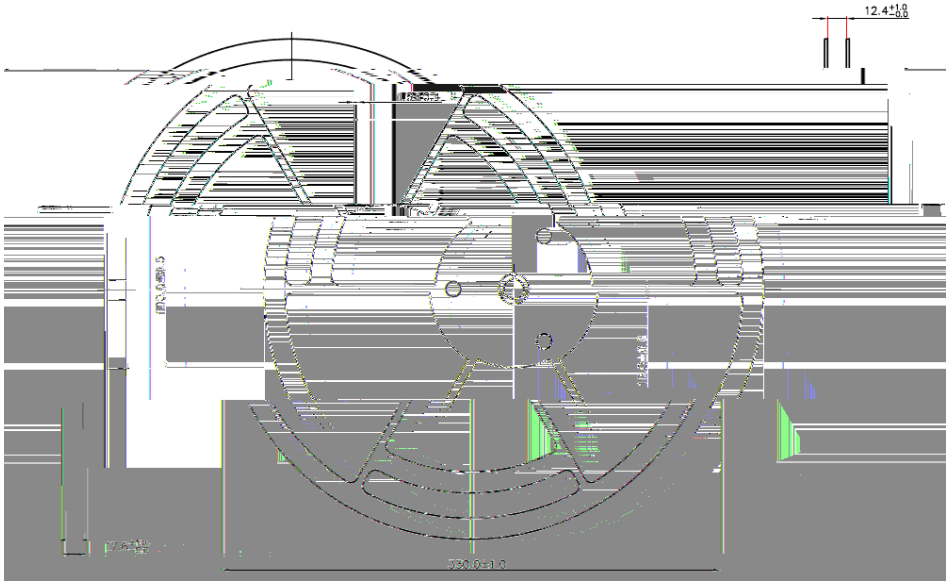
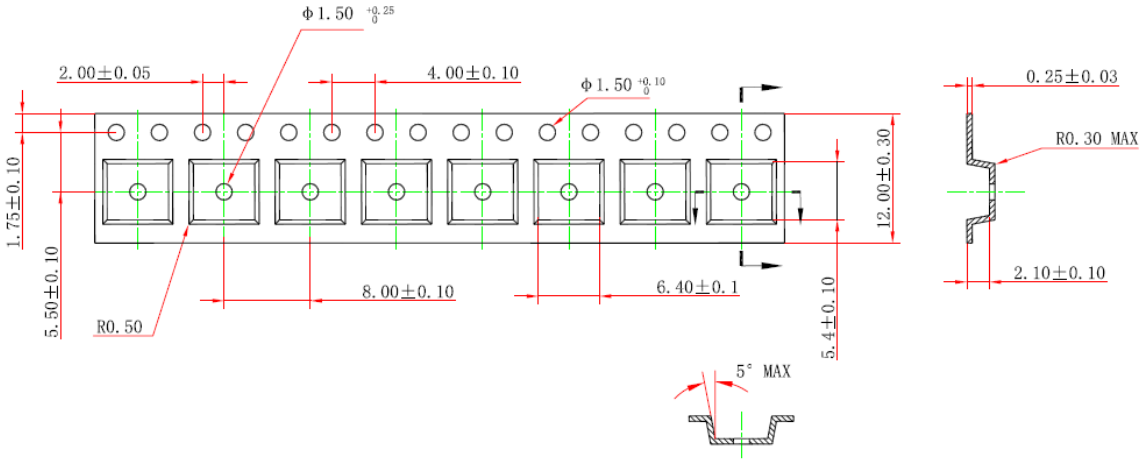
TAPE AND REEL INFORMATION





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