

2.8V-6V Vin 3A Synchronous Step Down Convertor

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C
 - Ambient Operating Temperature Range
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SCT2130Q

REVISION HISTORY

Revision 1.0: Release to production.

Revision 1.1: Update the accuracy range of V_{FB} .

Revision 1.2: Update the upper limits for I_Q , I_{SD} , V_{FB} , R_{HS} , and R_{LS} .

Revision 1.3: Update T_J in RECOMMENDED OPERATING CONDITIONS.

Revision 1.4: Update DEVICE ORDER INFORMATION and the parameter of $ILIM_{LS}$.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2130QFTAR	Tape & Reel	3000	130Q	8	FCQFN2x1.5-8

ELECTRICAL CHARACTERISTICS

$V_{IN}=5V$, $T_J=-40^{\circ}C\sim 125^{\circ}C$, typical values are tested under $25^{\circ}C$.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.8		6	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		2.7		V
	Hysteresis			175		mV
I_{SD}	Shutdown current			0.7	3	uA
I_Q	Quiescent current from V_{IN}	no load, no switching		1000	1400	uA
V_{FB}	Reference voltage of FB	$T_J=25^{\circ}C$	0.593	0.6	0.607	V
		$T_J=-40^{\circ}C\sim 125^{\circ}C$	0.591		0.607	V
I_{FB}	FB pin leakage current				100	nA
V_{UVP}	Undervoltage protection of reference voltage			433		mV
Power switch						
R_{HS}	High-side switch on resistance			25	48	m
R_{LS}	Low-side switch on resistance			20	38	m
$ILIM_{HS}$	High-side peak current limit		3.8	4.5	5.2	A
$ILIM_{LS}$	Low-side valley current limit		3.05	3.5		A
Soft start						
I_{SS}	Soft-start Current			3		uA
R_{SS}	SS pull down resistance			85		
EN & PG						
V_{ENH}	High-level Threshold voltage		1.2			V
V_{ENL}	Low- level Threshold voltage				0.4	V
R_{EN}	EN Pull down resistance			2		M
R_{DIS}	Output Discharge resistance			80		
V_{PGTL}	Power Good Lower Threshold voltage					

TYPICAL CHARACTERISTICS

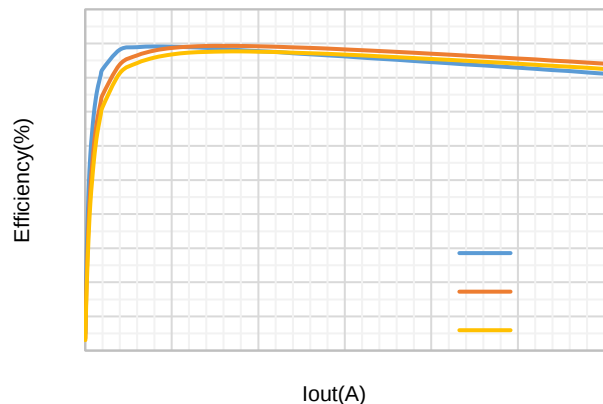


Figure 1. Efficiency vs Load Current, Vout=1.2V

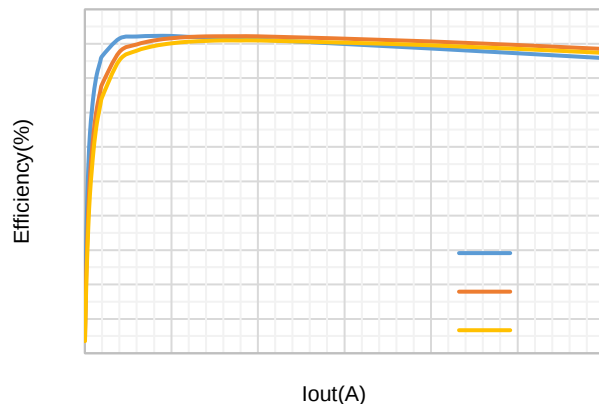


Figure 2. Efficiency vs Load Current, Vout=1.8V

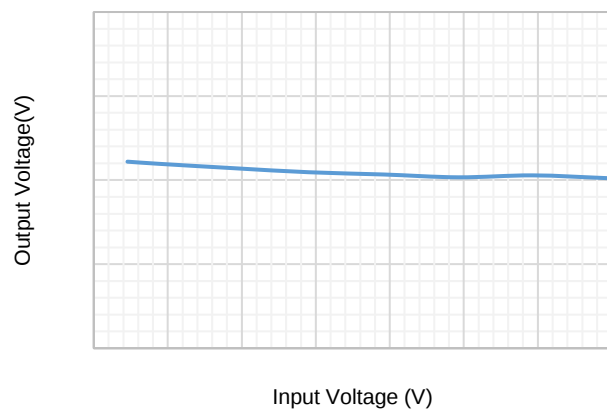


Figure 3. Line Regulation, Io=1.5A

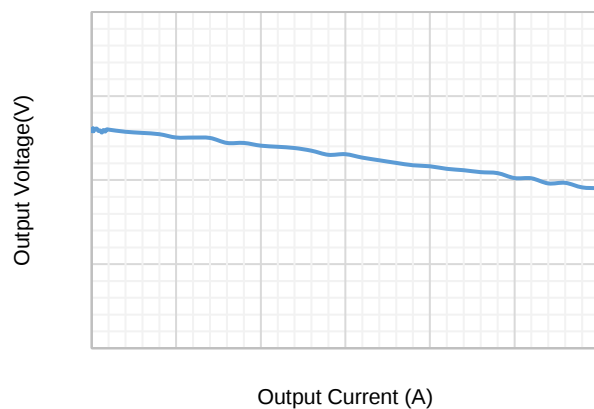


Figure 4. Load Regulation, Vin=5V

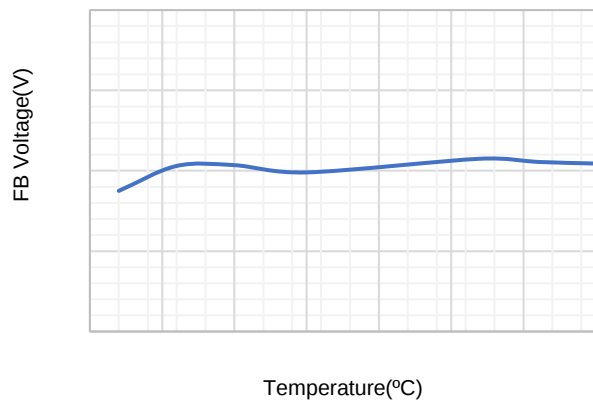


Figure 5. V_{FB} vs Temperature

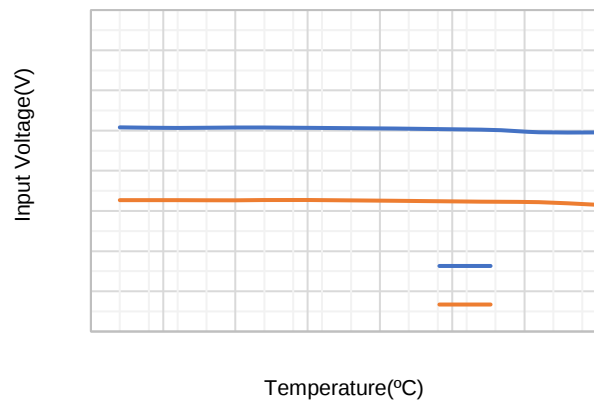


Figure 6. UVLO vs Temperature

OPERATION

Overview

The SCT2130Q is a 2.8V-6V input, 3A output, synchronous buck converter with built-in 25mΩ high-side and 20mΩ $R_{ds(on)}$ low-side power MOSFETs. It implements constant on time control to regulate output voltage, providing excellent line and load transient response, and internal error amplifier integrated improve the line and load regulation.

The switching frequency is fixed 2.1MHz. The SCT2130Q features programmable soft start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The SCT2130Q operates in Forced Continuous Conduction Mode (FCCM) to achieve low light load ripple. The quiescent current is typically 1000uA under no load and no switching.

The SCT2130Q full protection features include the input under-voltage lockout, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Constant On-time Control

Constant on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time -by-cycle based to maintain a pseudo-fixed frequency over the input voltage range. SCT2130Q turns off high-side MOSFET after the fixed-on time and turns on the low-side MOSFET. SCT2130Q turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following Equation 1:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \cdot f_s} \quad (1)$$

Where:

- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.
- f_s is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.6V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 100ns typical.

Under Voltage Lockout UVLO

The SCT2130Q Under Voltage Lock Out (UVLO) default startup threshold is typical 2.7V with VIN rising and shutdown threshold is 2.525V with VIN falling.

Enable (EN) and VOUT discharge

EN is a digital control pin that can turn the regulator on and off. When EN is pulled below the falling threshold voltage (0.4V), the chip shuts down. Force EN above its rising threshold voltage (1.2V) to turn the part on. Leave EN floating or pull it down to ground to disable the SCT2130Q. There is an internal 2 ground.

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When the device is disabled, the part automatically goes into output discharge mode, and its internal discharge MOSFET in VOUT pin provides a discharge path for the output capacitor.

Output Voltage

The SCT2130Q regulates the internal reference voltage at 0.6V. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 2 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$\text{---} \quad (2)$$

Where:

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Soft Start (SS)

The SCT2130Q has an external soft start (SS) pin that ramps up the output voltage at a controlled slew rate to the SS capacitor. tss can be calculated with Equation 3:

$$\text{---} \quad (3)$$

Where:

- C_{ss} is the external SS capacitor.
- I_{ss}

The minimum SS capacitor is recommended to be 1nF.

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the high-side MOSFET during the ON period and the low-side MOSFET during the OFF period. When the inductor current (I_L) reaches the high-side MOSFET peak current limit (typically 4.5A) during the ON period, the high-side MOSFET is forced off immediately to prevent the current from rising further. Then the low-side MOSFET turns on and stays on until I_L drops below the low-side MOSFET valley current limit (typically 3.5A). If output loading continues to increase, output will drop below the V_{UVP} , and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup -start period. If overload or hard short condition still exists during soft-start and make FB voltage lower than V_{UVP} , the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

Power Good Indicator

The SCT2130Q has one power good (PG) output to indicate normal operation after the soft-start time. PG is the open drain of an internal MOSFET, which has a maximum $R_{DS(ON)}$ below 2 Ω IN or an external voltage source through an external a resistor (e.g., MOSFET turns on, and PG is pulled to GND before soft start is ready. After V_{FB} reaches 95% of V_{REF} , PG is pulled high by the external voltage source with 80us delay. When V_{FB} drops to 90% or rises to 110% of V_{REF} , the PG

voltage is pulled to GND to indicate an output failure. If VIN and EN are not available, and PG is pulled up by an external power supply, PG will self-
-up resistor is used, the voltage on the pin is below 0.4V.

Thermal Shutdown

Once the junction temperature in the SCT2130Q exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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APPLICATION INFORMATION

Typical Application

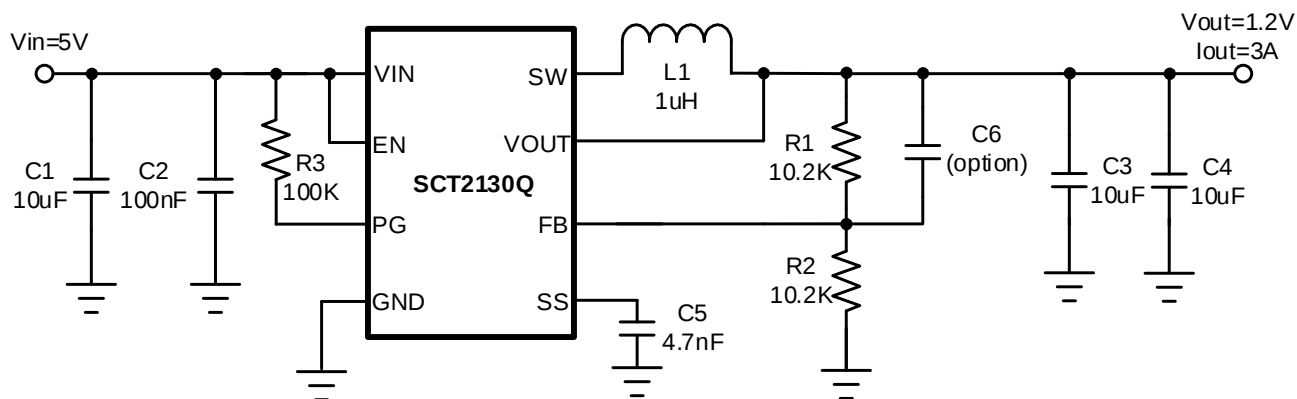


Figure 8. SCT2130Q Design Example, 1.2V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 2.8V to 6V
Output Voltage	1.2V
Maximum Output Current	3A
Switching Frequency	2.1MHz
Output voltage ripple (peak to peak)	2mV
Transient Response 0.3A to 2.7A load step	$V_{out} = 140\text{mV}$

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 10.2K . Use Equation 4 to calculate R1.

$$\text{---} \quad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.6V

Table 1. R₁, R₂ Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
1.2 V	10.2	10.2
1.8 V	20	10.2
3.3 V	46.5	10.2

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 10%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 5.

$$\text{---} \quad (5)$$

Where:

- I_{LPP} is the inductor peak-to-peak current.
- L is the inductance of inductor.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 6 to calculate the inductance value.

$$\text{---} \quad (6)$$

Where:

- L_{MIN} is the minimum inductance required.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN(max)}$ is the maximum input voltage.
- $I_{OUT(max)}$ is the maximum DC load current.
- LIR is coefficient of I_{LPP} to I_{OUT} .

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 7 and Equation 8.

$$\frac{I_{LPEAK}}{I_{LPP}} = \frac{I_{OUT}}{I_{LPP}} + \frac{I_{LPP}}{2} \quad (7)$$

$$I_{LPP} = \frac{I_{OUT}}{1 - D} + \frac{I_{LPP}}{2} \quad (8)$$

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 4.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 4.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2130Q can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g., 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 9.

$$I_{CRMS} = \frac{I_{OUT}}{2} \sqrt{\frac{1-D}{D}} \quad (9)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$(10)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 11 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN}} \left(\frac{1-D}{D} \right) \quad (11)$$

For this example, 10 μ F, X7R ceramic capacitors rated for 16 V in parallel are used. And a 0.1uF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 12 desired.

(12)

Where:

- ΔV_{OUT} is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to ΔV_{OUT} degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 10

Table 2: Component List with Typical Output Voltage BOM list

					option
					option

Application Waveforms

$V_{IN}=5V$, $V_{OUT}=1.2V$, unless otherwise noted

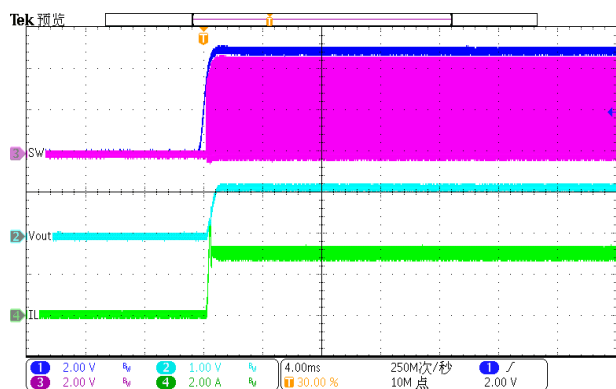


Figure 9. Power up ($I_{LOAD}=3A$)

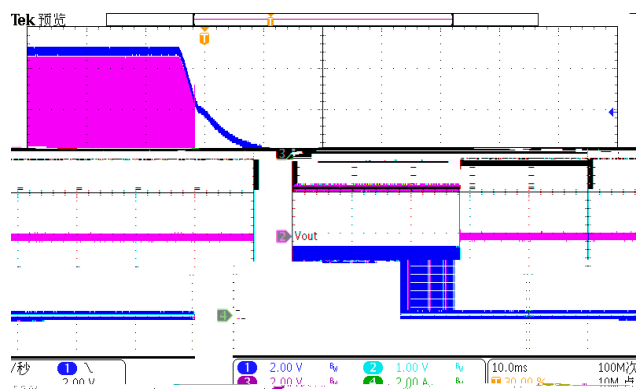


Figure 10. Power down ($I_{LOAD}=3A$)

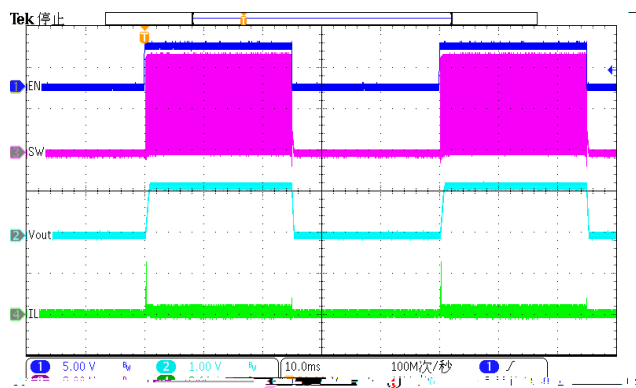


Figure 11. EN toggle ($I_{LOAD}=0.1A$)

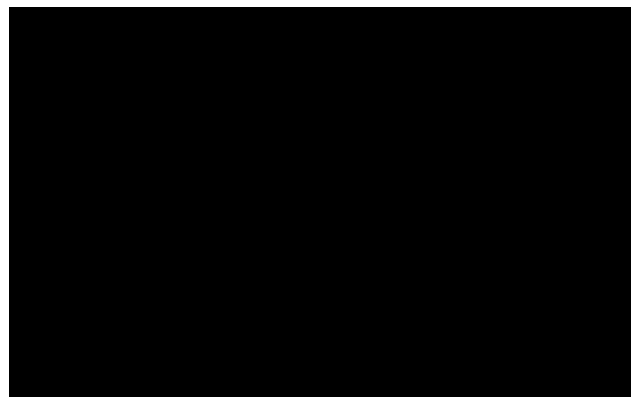


Figure 12. EN toggle ($I_{LOAD}=3A$)

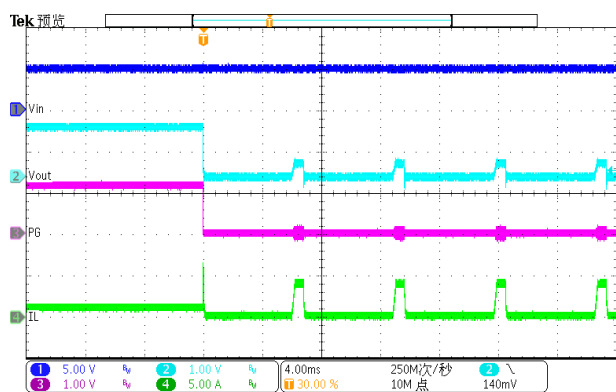


Figure 13. Over Current Protection (1A to hard short)

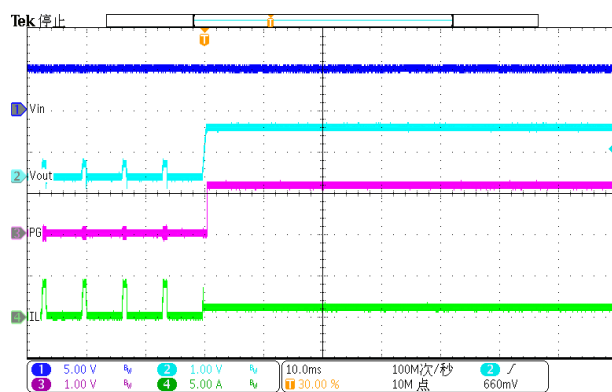


Figure 14. Over Current Release (hard short to 1A)

Application Waveforms

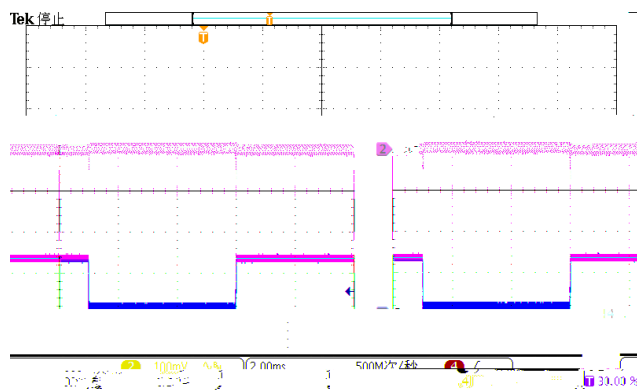


Figure 15. Load Transient (0.3A-2.7A, 1.6A/us)

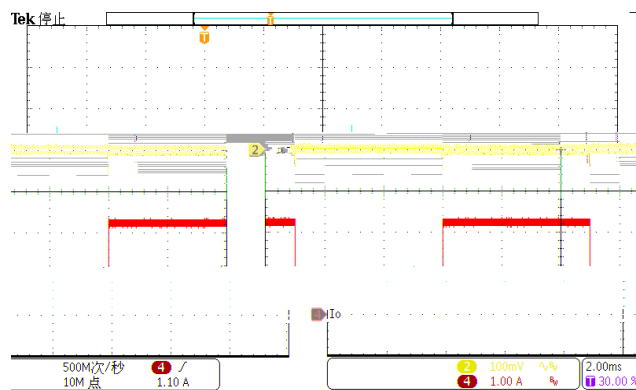


Figure 16. Load Transient (0.75A-2.25A, 1.6A/us)

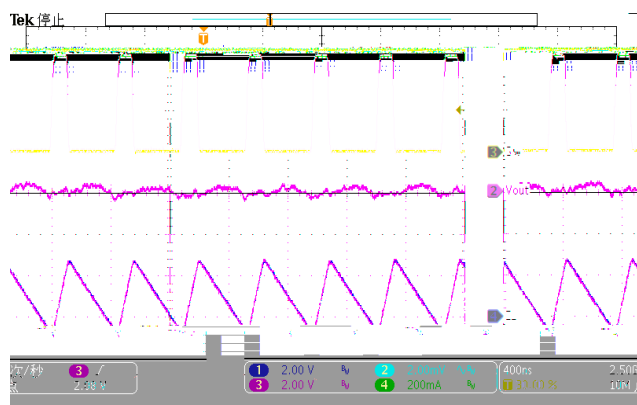


Figure 17. Output Ripple ($I_{LOAD}=100mA$)

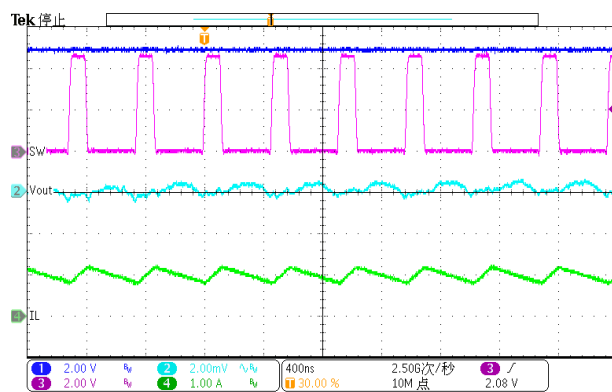


Figure 18. Output Ripple ($I_{LOAD}=1A$)

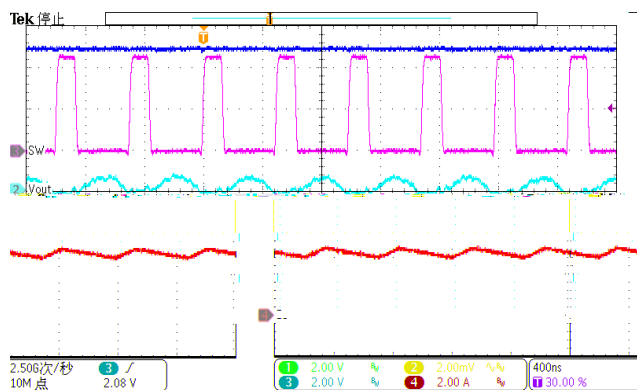


Figure 19. Output Ripple ($I_{LOAD}=3A$)



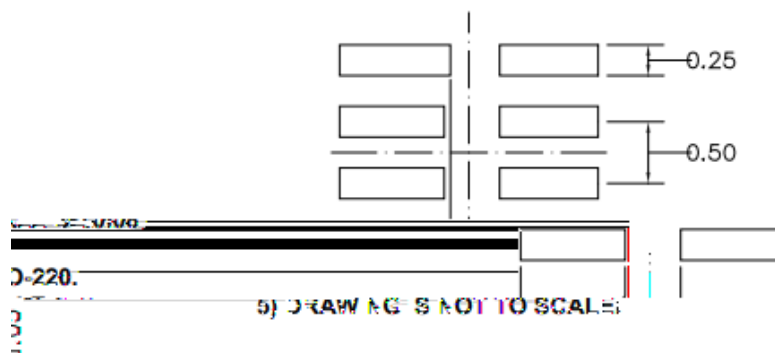
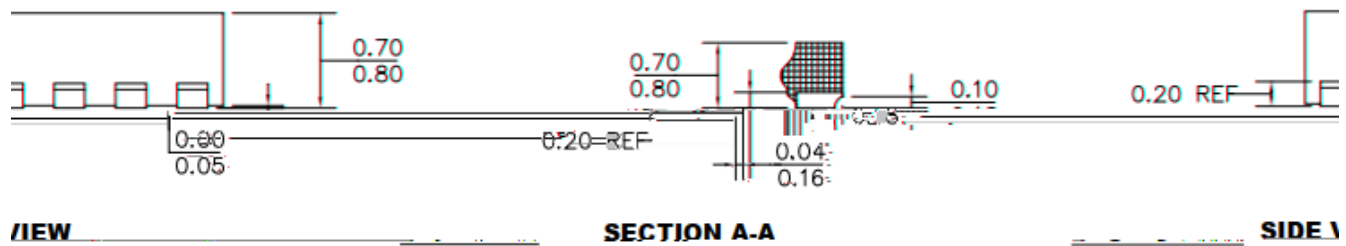
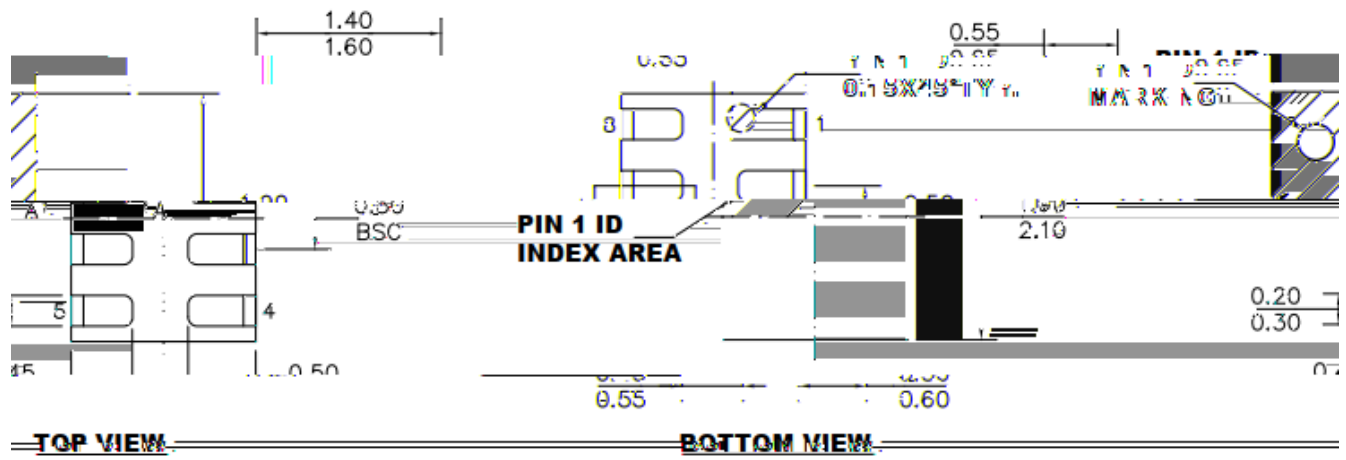
Figure 20. Thermal, $V_{IN}=5V$, $V_{OUT}=1.2V$, $I_{LOAD}=3A$

Layout Guideline

Proper PCB layout is a critical for SCT2130Q operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

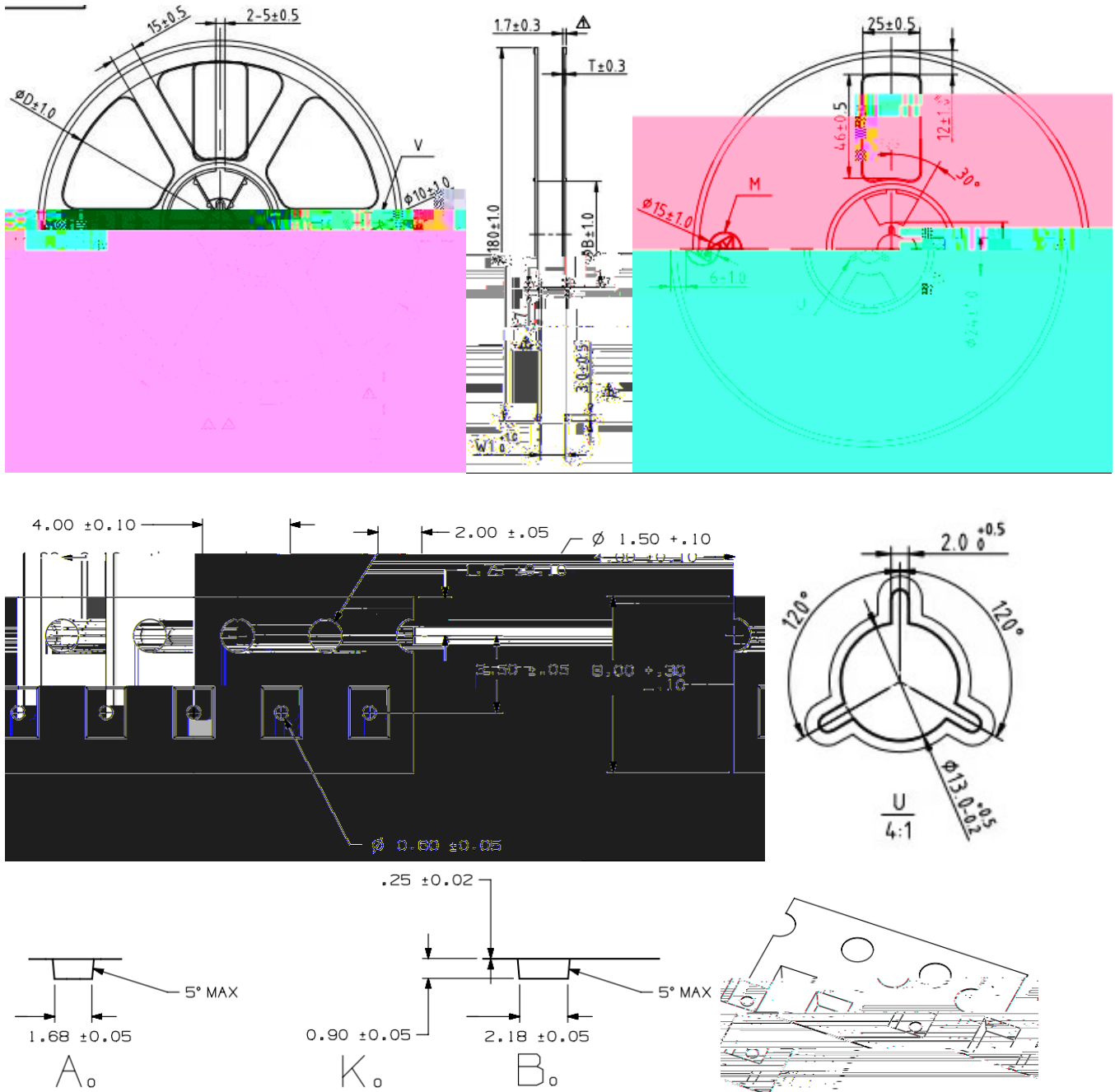
1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impedance and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the

PACKAGE INFORMATION

**NOTE:**

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPPLANABILITY SHALL BE 0.02 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.

TAPE AND REEL INFORMATION



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