- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide Input Voltage Range: 3.2V-50V
- Low Shutdown Current 3.7uA
- Low Quiescent operating Current: 450uA
- Adjustable Switching Frequency: 100KHz to 2.2MHz
- Integrated Frequency Dithering for EMI Mitigation
- External Frequency Synchronic
- External Compensation
- Supports additional Slope Compensation
- 22ms Internal Soft-start Time
- Integrated Protection Feature
  - Constant Peak-Current Protection Threshold Over Input Voltage
  - Output Overvoltage Protection
  - Adjust Under-Voltage Lockout
  - Optional Hiccup Over Load Protection
  - Thermal Shutdown Protection:165°C
- MSOP-8L(3mm*3mm) Package

- Muti-output Flyback
- LED Bias Supply
- Portable Speaker Supply
- Battery Powered Boost/Flyback/SEPIC application

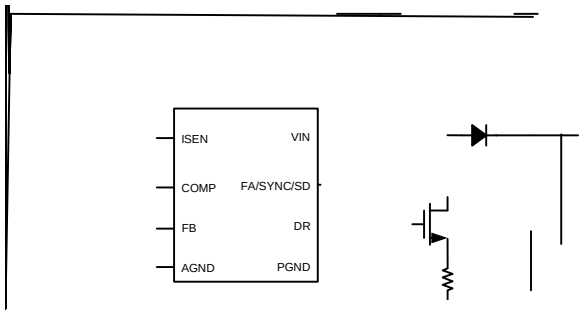
The SCT81620Q device is a wide input, non-synchronous boost controller. The Device can be used in Boost, SEPIC and Flyback converters and topologies.

The switching frequency of the SCT81620Q device can be adjusted to any value between 100kHz and 2.2MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit is adjustable through an external resistor.

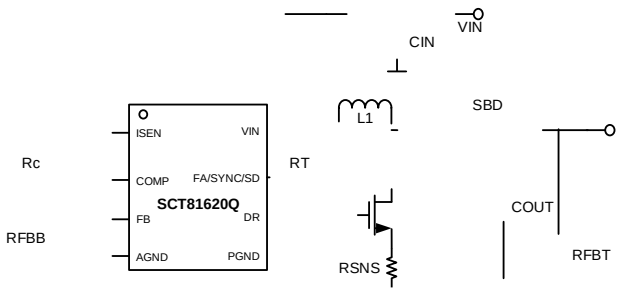
The SCT81620Q is an Electromagnetic Interference (EMI) friendly controller with implementing optimized design for EMI reduction. The SCT81620Q features Frequency Spread Spectrum (FSS) with ±6% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT81620Q device has built-in protection features such as thermal shutdown, short-circuit protection and overvoltage protection. Power-saving shutdown mode reduces the total supply current to 3.7 μA. Integrated current slope compensation simplifies the design and, if needed for specific applications, can be increased using a single resistor.

The device is available in a MSOP-8L(3mm*3mm) Package.



BOOST



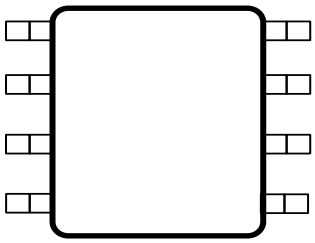
SEPIC

Revision 1.1: Update Device Order Information

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT81620QMTDR	Tape & Reel	4000	1620Q	8	8-Lead 3mm×3mm Plastic MSOP

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	62	V
DR	-1	6.6	V
ISEN, COMP, FB, FA/SYNC/SD	-5	5.5	V
Peak Driver Output Current		1(2)	A
Junction temperature(2)	-40	150	C
Storage temperature T_{STG}	-65	150	C



Top View: 8-Lead Plastic MSOP 3mmx3mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) Guaranteed by design, not tested in productions.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

NAME	NO.	DESCRIPTION
ISEN	1	Current sense input pin. Connect to the positive side of the current sense resistor through a short path.
COMP	2	Output of the internal transconductance error amplifier. Connect the loop compensation components between this pin and GND.
FB	3	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage. The device regulates FB voltage to the internal reference value of 1.26V typical.
AGND	4	Analog ground pin.
PGND	5	Power ground pin.
DR	6	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
FA/SYNC/SD	7	Switching frequency setting pin. The switching frequency is programmed by a single resistor between this pin and AGND. The internal clock can be synchronized to an external clock. A high level on & will then draw 3.7 µA from the supply typically.

VIN	8	Power supply input pin

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.2	50	V
V_{CC}	VCC voltage range	3.2	6.1	V
T_J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins	-1	+1	kV

PARAMETER	THERMAL METRIC	MSOP-8	UNIT
R	Junction to ambient thermal resistance(1)	132.8	°C/W
R (top)	Junction to case (top) thermal resistance(1)	64.1	°C/W
R B	Junction to board thermal resistance(1)	83.8	°C/W

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT81620Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT81620Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.92		60	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.9 160		V mV
I_{SD}	Shutdown current	$V_{FA/SYCN/SD}$=5V		3.7	8	uA
I_Q	Quiescent current from VIN	no load, no switching		460		uA
Reference and Control Loop						
V_{REF}	Reference voltage of FB	Tj=25°C	1.241	1.26	1.278	V
		Tj=-40~125°C	1.222		1.297	
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V	500	700	900	uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V	120	155	195	

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Protection						
V_{OVTH}(3)	FB overvoltage threshold	FB rising	25	85	135	mV
		Hysteresis	30	80	130	mV
T_{SD}(1)	Thermal shutdown threshold	T_J rising		165		°C
	Hysteresis			25		°C

(1) Guaranteed by design and bench, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) The overvoltage protection is specified with respect to the feedback voltage. This is because the overvoltage protection tracks the feedback voltage. The overvoltage threshold can be calculated by adding the feedback voltage (V_{FB}) to the overvoltage protection specification.

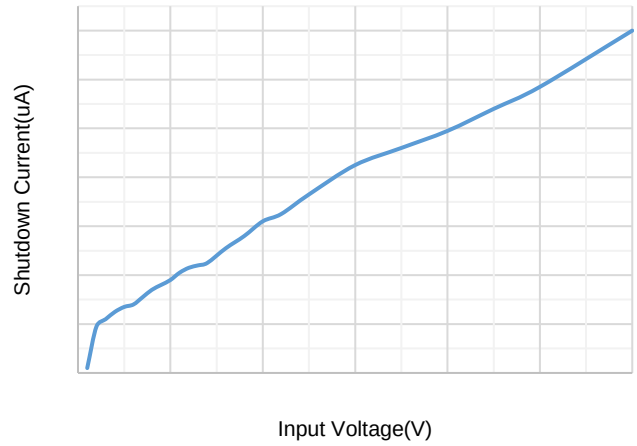


Figure 1. ISD vs Input Voltage

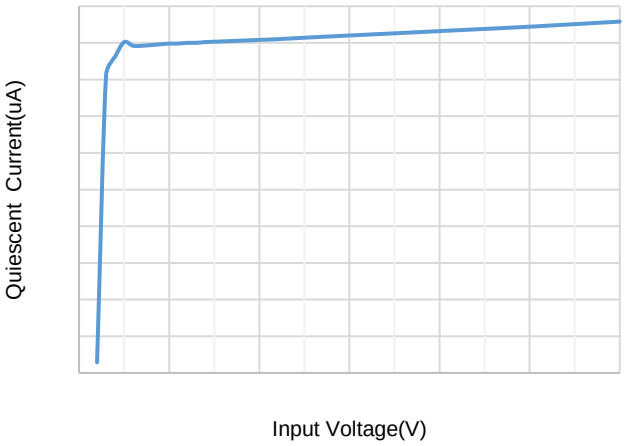


Figure 2. IQ vs Input Voltage

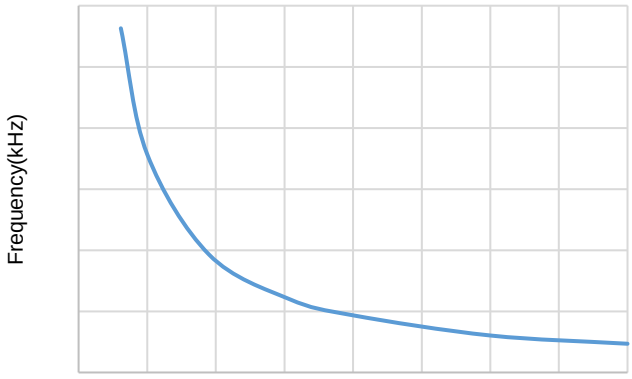


Figure 3. Switching Frequency vs RT

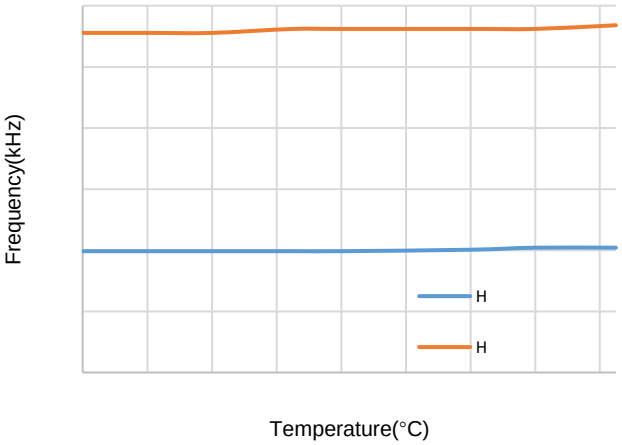


Figure 4. Switching Frequency vs Temperature

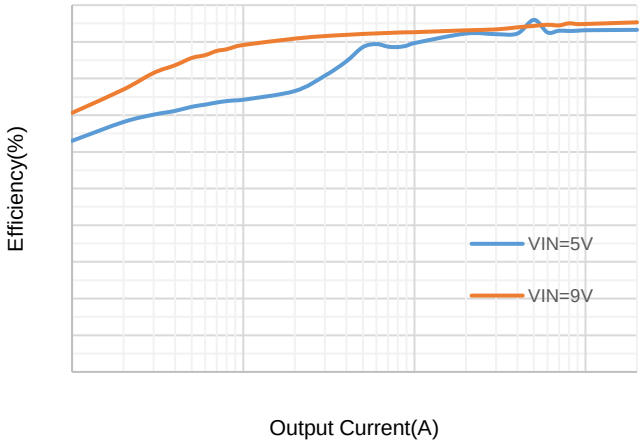


Figure 5. Efficiency vs Load Current, Boost, VOUT=12V

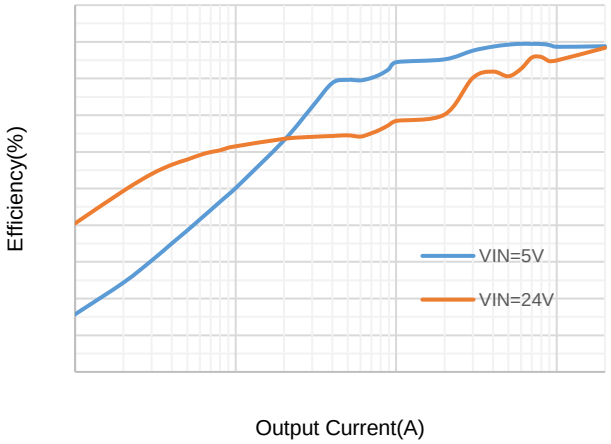


Figure 6. Efficiency vs Load Current, Sepic, VOUT=12V

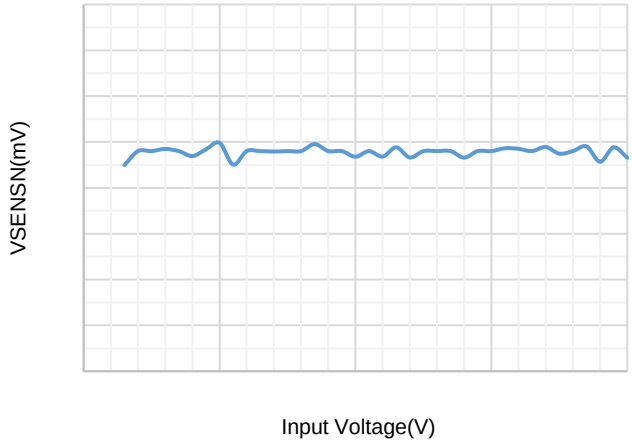


Figure 7. VSENSN vs Input Voltage

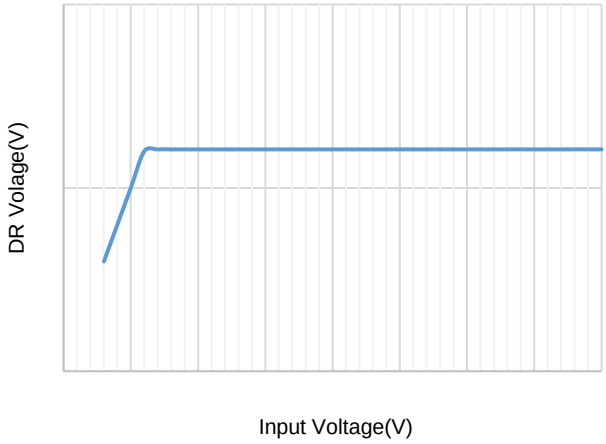


Figure 8. DR Volage vs Input Voltage

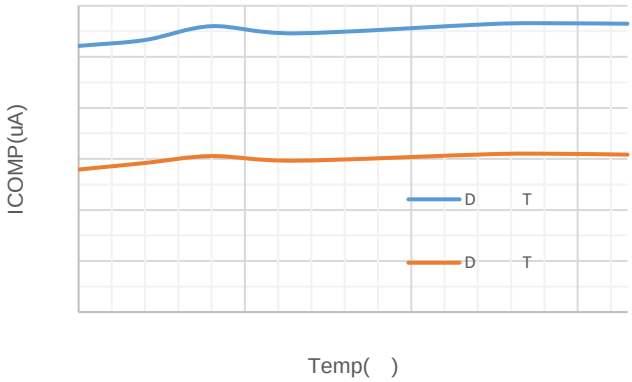


Figure 9. COMP Current vs Temperature

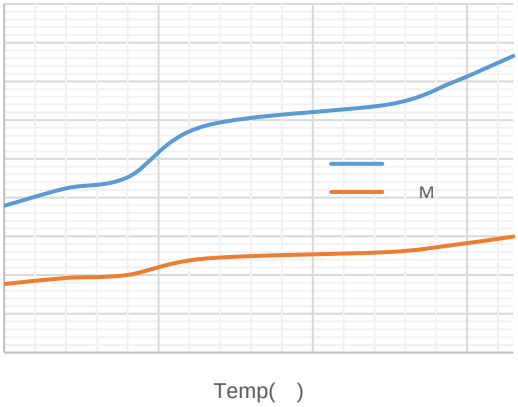


Figure 10. DR Resistance vs Temperature

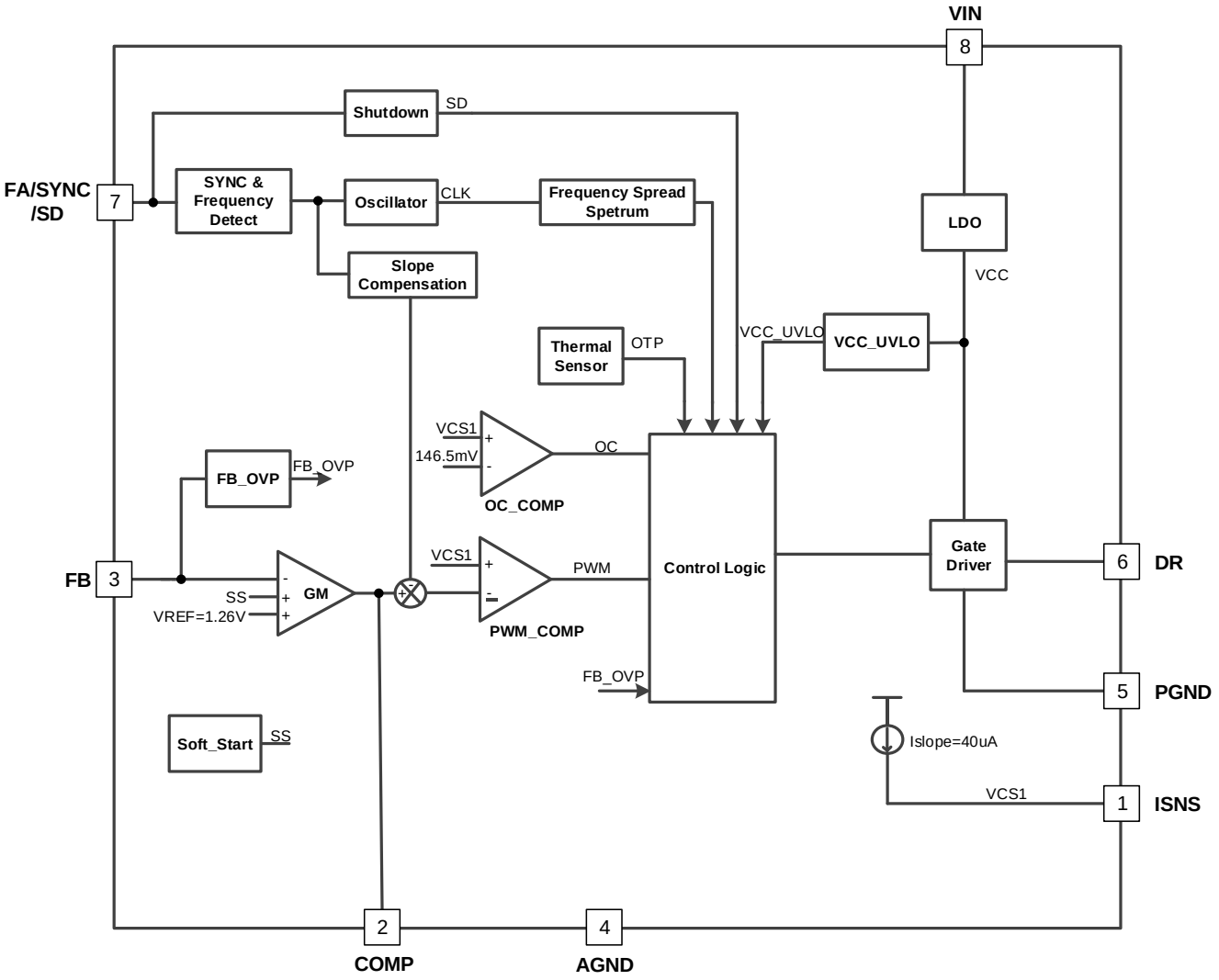


Figure 11. Functional Block Diagram

Overview

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Overvoltage Protection

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Slope Compensation Ramp

The SCT81620Q uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. However, current mode control has a Sub-harmonic Oscillation when duty cycles greater than 50%. To prevent the Sub-harmonic oscillations, a compensation ramp is added to the control signal.

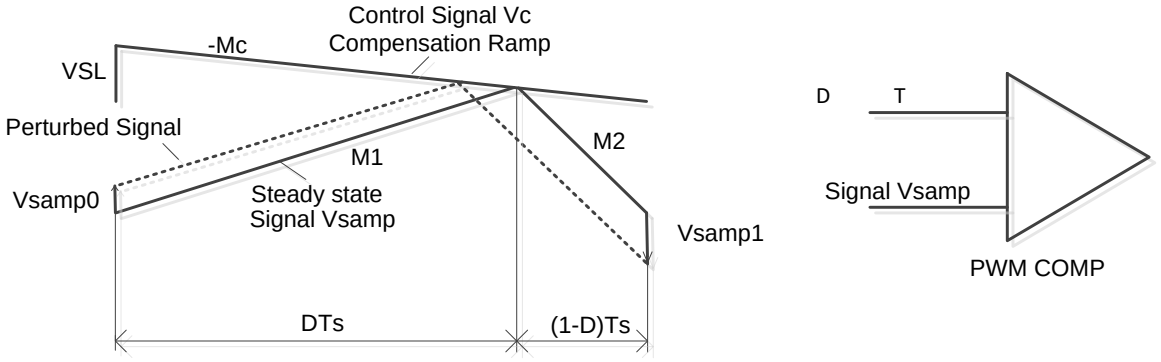

Figure12. Sub-Harmonic Oscillation for D>0.5 and Compensation Ramp to Avoid Sub-Harmonic Oscillation

$$V_{samp} = I_L * R_{SEN} \quad (1)$$

% %

%

$$M_1 = M_{on} * R_{SEN} \quad (2)$$

$$-M_2 = -M_{off} * R_{SEN} \quad (3)$$

$$M_1 = M_{on} * R_{SEN} = Vin * R_{SEN} / L \quad (4)$$

$$M_2 = M_{off} * R_{SEN} = (Vout - Vin) * R_{SEN} / L \quad (5)$$

$$\Delta V_{samp1} = -(\frac{M_2 - M_c}{M_1 + M_c}) * \Delta V_{samp0} \quad (6)$$

$$\Delta V_{samp1} = -(\frac{M_2}{M_1}) * \Delta V_{samp0} = -(\frac{D}{1-D}) * \Delta V_{samp0} \quad (7)$$

(

$$\left| -(\frac{M_2 - M_c}{M_1 + M_c}) \right| < 1 \quad (8)$$

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$$M_c = V_{SL} * F_s \quad (9)$$

&

) %

$$M_c = (V_{SL} + K * R_{SL}) * F_s \quad (10)$$

'

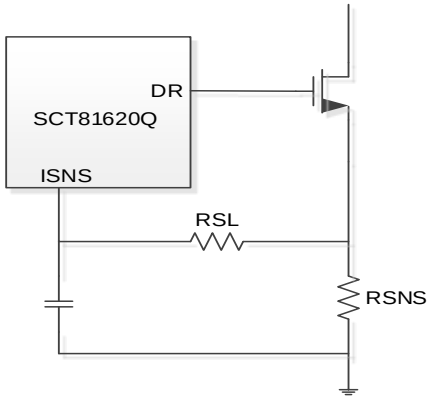

Figure13 .External RSL to increase slope compensation

Adjustable Peak Current Limit

$$I_{PEAK\_CL} \quad \frac{V_{SENSE} \quad 40uA \quad R_{SL} \quad D}{R_{SNS}} \qquad (11)$$

Where

- VSENSE is ISEN pin limiting voltage (Typ.=146.5mV)
- IPEAK-CL is the inductor peak current limit
- RSL is Slope compensation resistor
- D is Duty cycle
- RSNS is the Inductance peak current detection resistance

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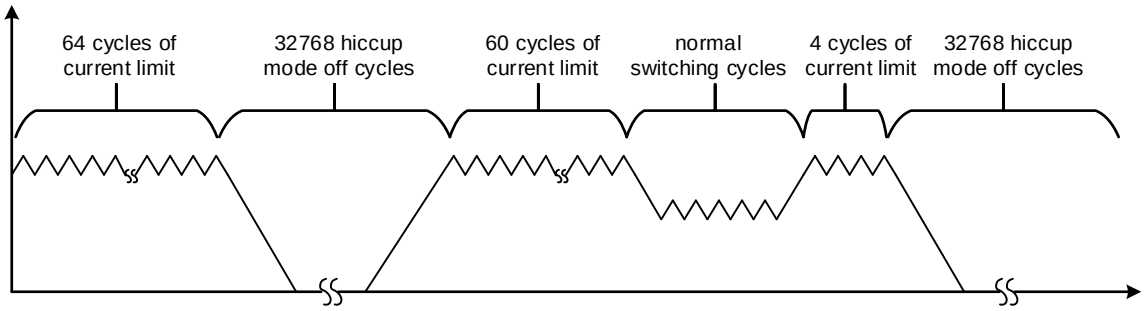

Figure14. Hiccup Mode Protection

Output Voltage

%

%

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (12)$$

where:

- V_{REF} is the feedback reference voltage, typical 1.26V

Frequency Adjust/Shutdown/ Synchronization

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$$R_{FA}(k\Omega) = \frac{19700}{fsw(kHz)} - 1.177 \quad (13)$$

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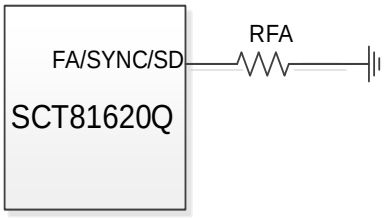

Figure15. Frequency Adjust

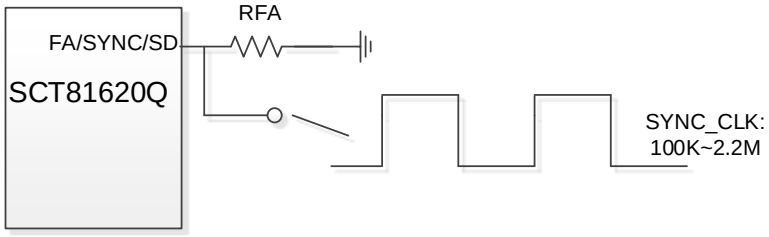

Figure16. Frequency Sync

Typical Application (Boost)

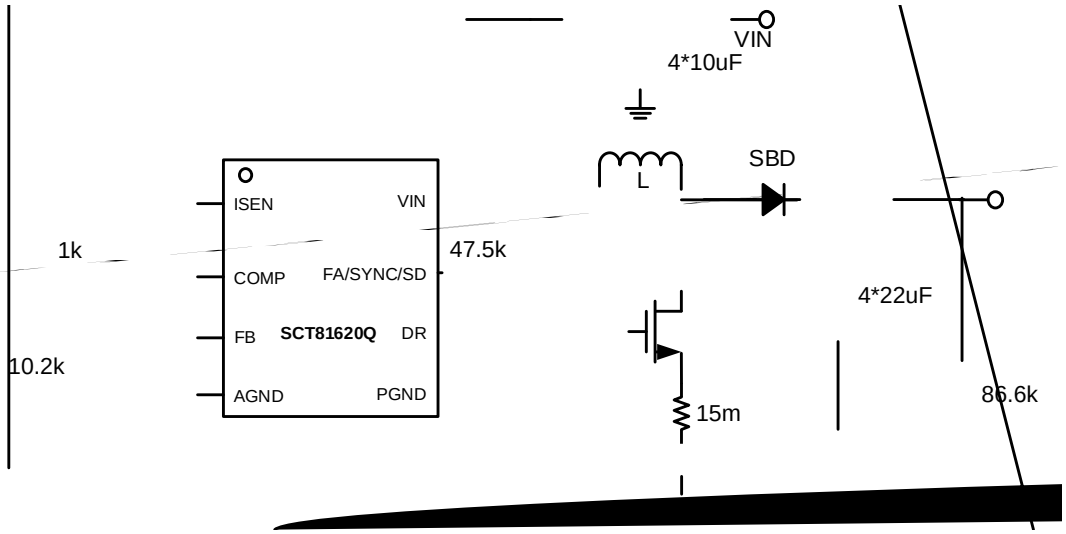

Figure 19. Application Schematic, 3V to 11V, 2A Boost Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 3V to 11V
Output Voltage	12V
Maximum Output Current	3A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

Inductor Selection (Boost)

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$$\frac{C}{C} \quad (14)$$

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
-

(

$$\frac{2}{\quad} \quad (15)$$

Where

- I_{LPP} is the inductor peak-to-

'

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%%

Where

I_G is the gate drive current.

Output Diode Selection

%

$$I_{D(PEAK)} = \frac{I_{OUT}}{(1-D)} + \Delta I_L \quad (24)$$

Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

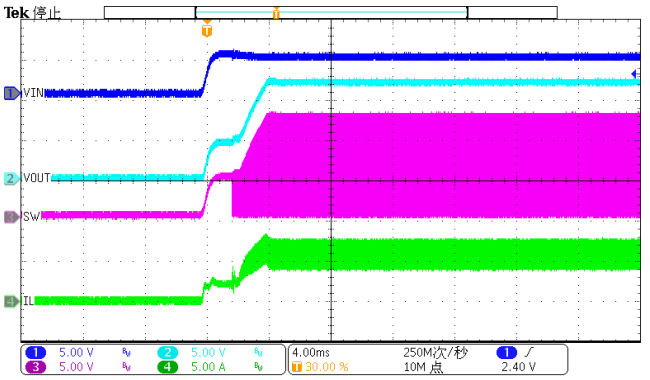


Figure 20. Power up(Iload=2A)

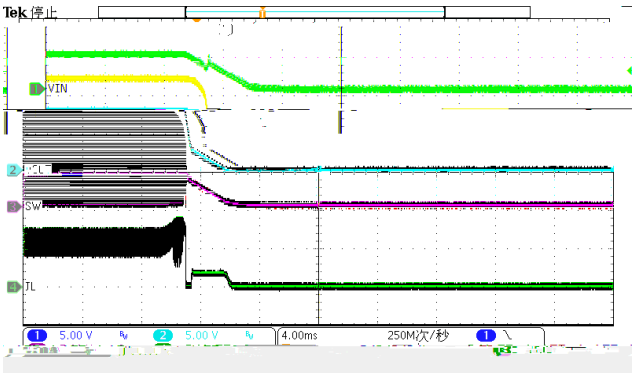


Figure 21. Power down(Iload=2A)

Figure 22. Over current protection (Iload=5A)

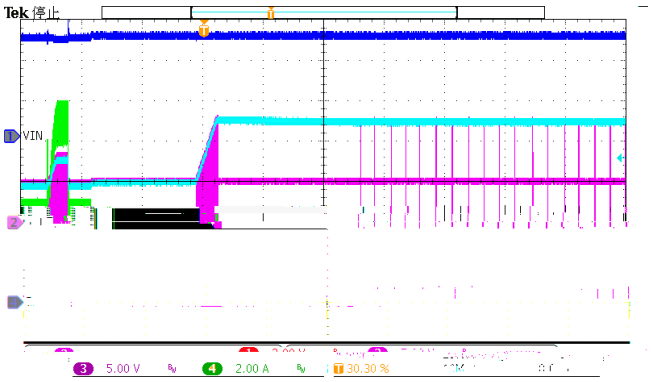


Figure 23. Over current recovery (Iload=5A)

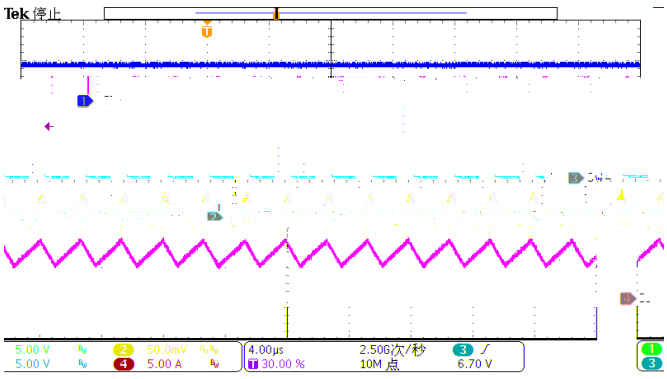


Figure 24. Steady-state (Iload=2A)

Figure 25. Sync Frequency

Typical Application (Sepic)

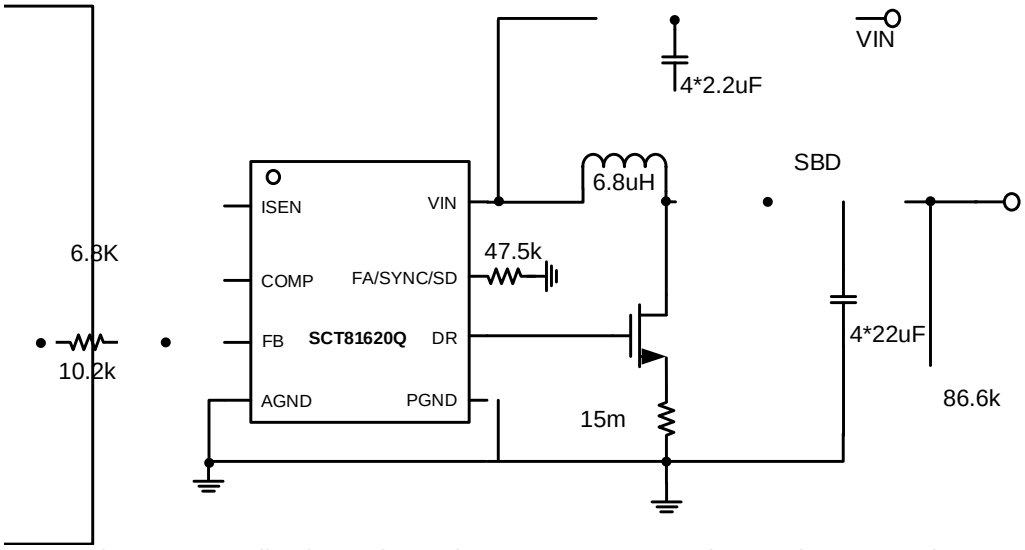


Figure 26. Application Schematic, 5V to 50V, 2A Sepic Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 5V to 50V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

Inductor Selection (Sepic)

% '
%

$$\Delta I_{L1} = I_{IN} \times 40\% = I_O \times \frac{V_O}{V_{IN\_MIN}} \times 40\% \quad (25)$$

$$\Delta I_{L2} = I_O \times 40\% = I_O \times 40\% \quad (26)$$

%

$$L_1 = L_2 = L = \frac{V_{IN\_MIN}}{\Delta I_L \times f_{SW}} \times D_{MAX} \quad (27)$$

- f_{SW} is the switching frequency.

$$I_{L1\_PEAK} = I_{IN} + \frac{\Delta I_L}{2} = I_O \times \frac{V_O}{V_{IN\_MIN}} \times (1 + \frac{40\%}{2}) \quad (28)$$

$$I_{L2\_PEAK} = I_O + \frac{\Delta I_L}{2} = I_O \times (1 + \frac{40\%}{2}) \quad (29)$$

%

$$L_1 = L_2 = \frac{L}{2} = \frac{V_{IN\_MIN}}{2 \times \Delta I_L \times f_{SW}} \times D_{MAX} \quad (30)$$

Power MOSFET Selection

$$V_{SW\_PEAK} = V_{IN} + V_O + V_D \quad (31)$$

$$I_{Q\_PEAK} = I_{L1\_PEAK} + I_{L2\_PEAK} \quad (32)$$

$$I_{Q\_RMS} = I_O \times \sqrt{\frac{\left(V_O + V_{IN\_MIN} + V_D\right) \times \left(V_O + V_D\right)}{V_{IN\_MIN}^2}} \quad (33)$$

$$P_{DIS} = I_{Q\_RMS}^2 \times R_{DS\_ON} \times D_{MAX} + \left(V_O + V_{IN\_MIN}\right) \times I_{Q\_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \quad (34)$$

- *I_G is the gate drive current.*

$$I_{COUT\_RMS} = I_O \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} \quad (41)$$

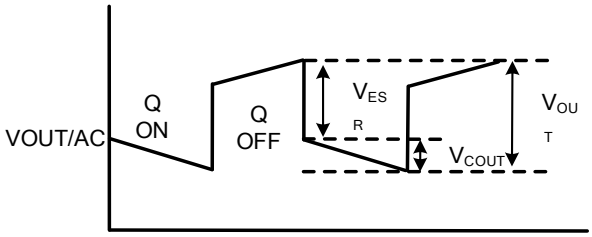


Figure 27. Output Voltage Ripple

Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

Figure 28. Power up(Iload=2A)

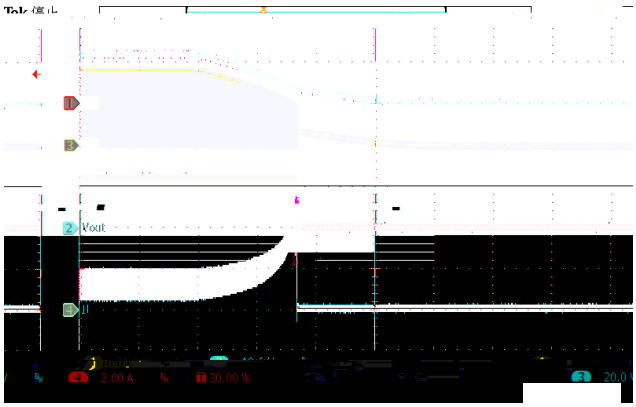


Figure 29. Power down(Iload=2A)

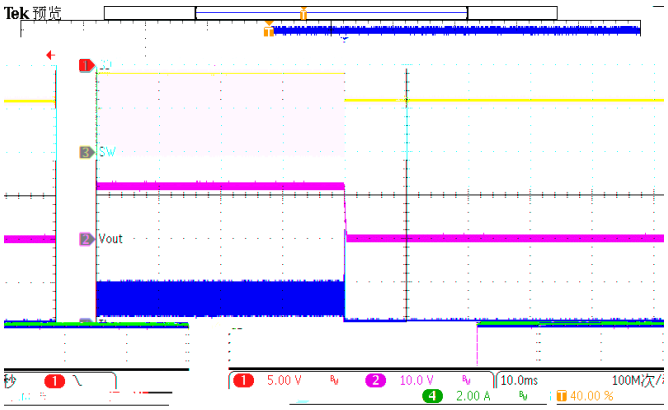


Figure 30. Shutdown remove

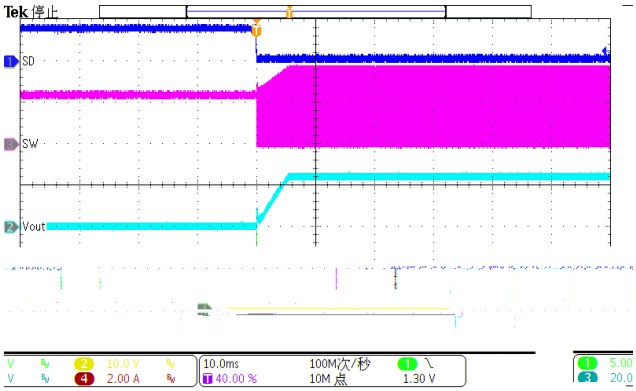


Figure 31. Shutdown remove

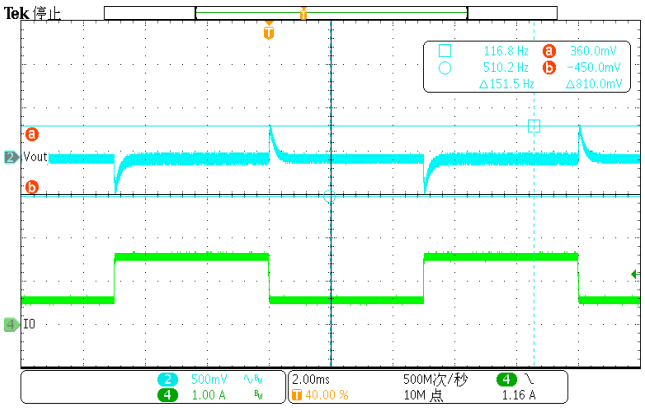


Figure 32. LoadTrans (Iload=0.5A-1.5A)

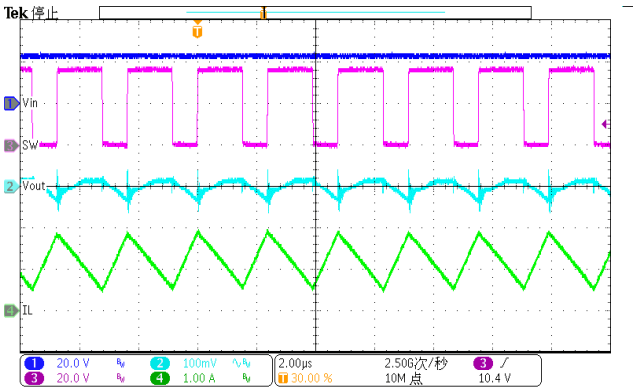


Figure 33. steady-state (Iload=2A)

Layout Guideline

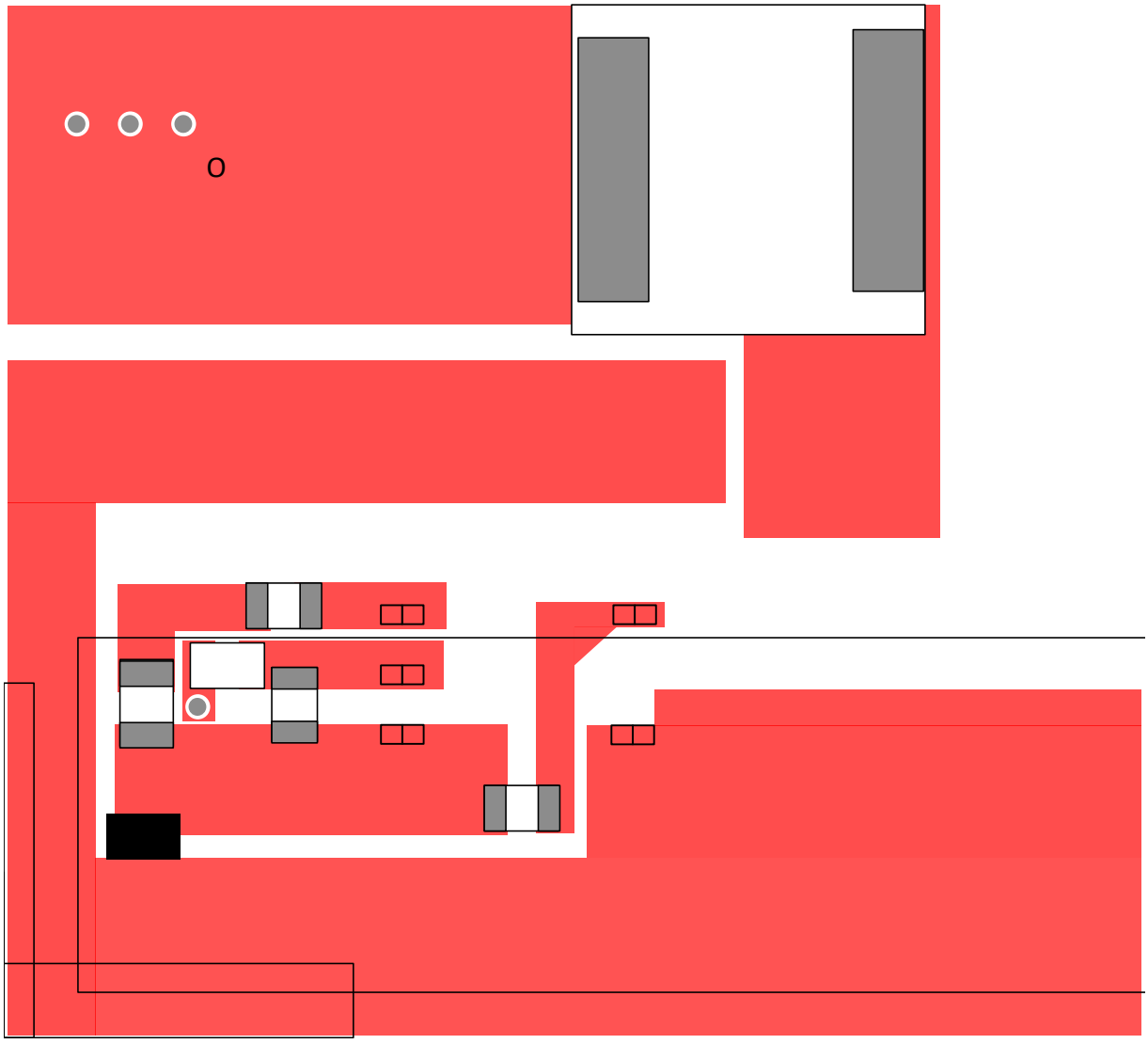
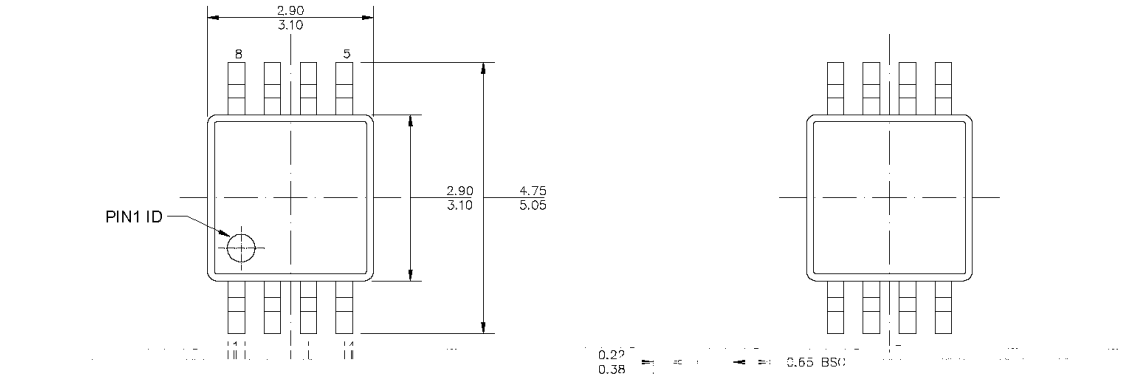
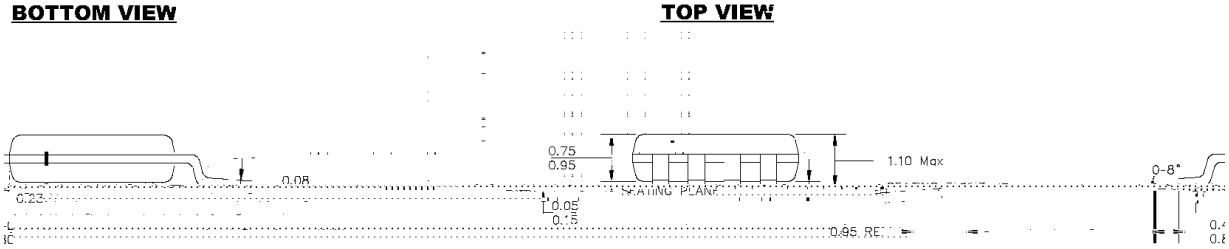


Figure 34. BOOST PCB Layout



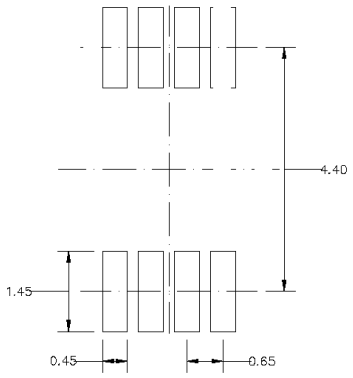
BOTTOM VIEW **TOP VIEW**



FRONT VIEW **SIDE VIEW**

LD

N BA.



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MO
FLASH, PROTRUSION OR GATE BURR.
3) DRAWING MEETS JEDEC MO-187, VARIATIO
4) DRAWING IS NOT TO SCALE.