- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide Supply Voltage Range: 4.5V - 24V
- 4A Peak Source Current and 4A Peak Sink Current
- Stackable Output for Higher Driving Capability
- Negative Input Voltage Capability: Down to -5V
- TTL Compatible Input Logic Threshold
- Propagation Delay: 13ns
- Typical Rising and Falling Times: 8ns
- Typical Delay Matching: 1ns
- Low Quiescent Current: 55uA
- Output Low When Input Floating
- Independent Enable Logic for Each Channel
- Thermal Shutdown Protection: 170°C
- Available in SOP-8 Package

- IGBT/MOSFET Gate Driver
- Variable Frequency-Drive (VFD)
- Switching Power Supply
- Motor Control
- Solar Power Inverter

The SCT52240Q is a wide supply, dual channel, high speed, low side gate drivers for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with rail-to-rail output capability. The 24V power supply rail enhances the driver output ringing endurance during the power device transition.

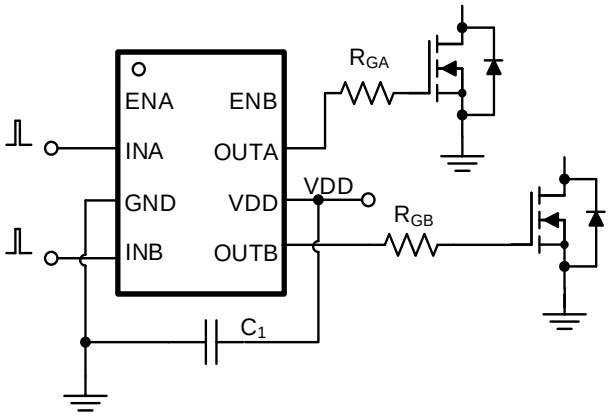
The minimum 13ns input to output propagation delay enables the SCT52240Q suitable for high frequency power converter application.

The SCT52240Q features wide input hysteresis that is compatible for TTL low voltage logic. The SCT52240Q has the capability to handle negative input down to -5V, which increases the input noise immunity.

The SCT52240Q has very low quiescent current that reduces the stand-by loss in the power converter. The SCT52240Q each channel driver adopts non-overlap driver design to avoid the shoot-through of output stage. The two channels INA and INB have critical propagation delay matching and artificial dead time implemented in output stage, which enable stackable output available when the system needs higher driving capability.

The SCT52240Q features 170°C thermal shut down. The SCT52240Q is available in SOP-8 package.

SCT52240Q Typical Application



Application Waveform

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to market

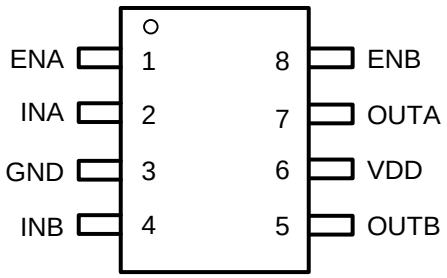
Revision 1.1: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT52240QSTDR	Tape & Reel	4000	2240Q	8	SOP-8L

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
ENA, ENB	-0.3	26	V
INA, INB	-5	26	V
OUTA, OUTB	-0.3	VDD+0.3	V
OUTA, OUTB (Pulse<0.2us)	-3	VDD+0.3	V
VDD	-0.3	26	V
Operating junction temperature TJ (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

Top View: SOP-8pin
Plastic



(1) Stresses beyond those listed under Absolut Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

NAME	NO.	PIN FUNCTION
ENA	1	Channel A enable logic input, TTL compatible. Floating logic high.
INA	2	Channel A logic input, TTL compatible. Floating logic low.
GND	3	Power ground. Must be soldered directly to ground plane for thermal performance improvement and electrical contact.
INB	4	Channel B logic input, TTL compatible. Floating logic low.
OUTB	5	Channel B gate driver output
VDD	6	Power Supply, must be locally bypassed by the ceramic cap.
OUTA	7	Channel A gate driver output
ENB	8	Channel B enable logic input, TTL compatible. Floating logic high.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5	24	V
$V_{INA,INB}$	Input voltage range	-5	24	
T_J	Operating junction temperature	-40	150	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

PARAMETER	THERMAL METRIC	SOP-8L	eMSOP-8	UNIT
R .	Junction to ambient thermal resistance (1)	130	72	°C/W
R .	Junction to case thermal resistance (1)	80	65	

(1) SCT provides R . and R . numbers only as reference to estimate junction temperatures of the devices. R . and R . are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT52240Q is mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT52240Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R . and R JC.

V_{DD}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{DD}	Operating supply voltage		4.5		24	V
V_{DD_UVLO}	Input UVLO Hysteresis	V_{DD} rising		4.2 300	4.5	V mV
I_Q	Supply current	EN=V_{DD}=3.5V, INA=INB=GND		55	115	uA
		EN=V_{DD}=12V, INA=INB=GND		120	190	uA
INPUTS						
V_{INA,INB_H}	Input logic high threshold			2.1	2.4	V
V_{INA,INB_L}	Input logic low threshold		0.8	1		V
V_{IN_Hys}	Hysteresis			1.1		V
V_{ENA,ENB_H}	Enable logic high threshold			2.1	2.4	V
V_{ENA,ENB_L}	Enable logic low threshold		0.8	1		V
V_{EN_Hys}	Hysteresis			1.1		V
OUTPUTS						
V_{DD_VOH}	Output output high voltage	I_{OUT}= - 10mA			150	mV
V_{OL}	Output low voltage	I_{OUT}= 10mA			10	mV
$I_{SINK/SRC}$	Output sink/source peak current(1)	C_{Load}=10nF, F_{SW}=1kHz		4		A
R_{OH}	Output pull high resistance (only PMOS ON)	I_{OUT}= - 10mA	5	9	18	
R_{OL}	Output pull low resistance	I_{OUT}= 10mA	0.3	0.6	1.2	
Timing						
T_R	Output rising time	C_{Load}=1nF		8	20	ns
T_F	Output falling time	C_{Load}=1nF		8	20	ns
T_{D_IN}	Input to output propagation delay, Rising edge		7	13	25	ns
	Input to output propagation delay, Falling edge		7	13	25	ns
T_{M_IN}	Input to output delay matching			1	4	ns
T_{MIN_ON}	Minimum input pulse width	C_{Load}=1nF		20	30	ns
Protection						
T_{SD}	Thermal shutdown threshold	T_J rising		170		°C
	Hysteresis			25		°C

(1)Guaranteed by design

V_{IN}=12V, T_A= 25°C.

Figure 1. UVLO vs Temperature

Figure 2. Supply current vs Temperature

Figure 3. Input Threshold vs Temperature

Figure 4. Enable Threshold vs Temperature

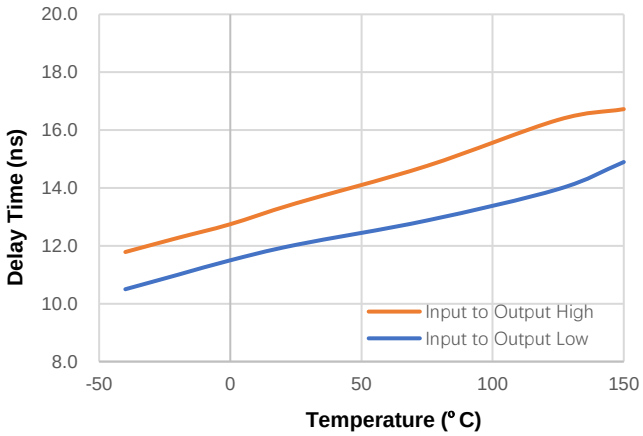


Figure 7. Input to Output Propagation Delay vs Temperature

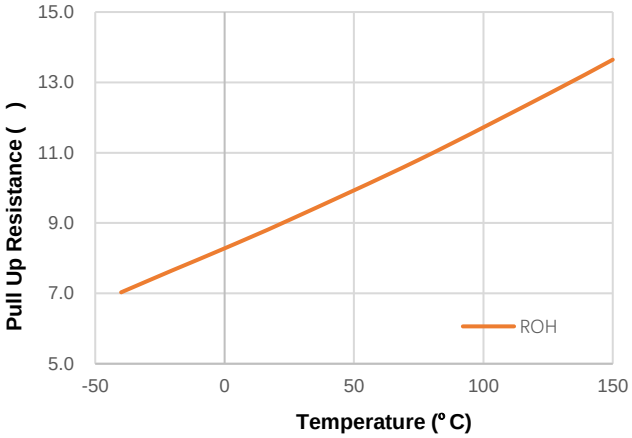


Figure 8. ROH vs Temperature

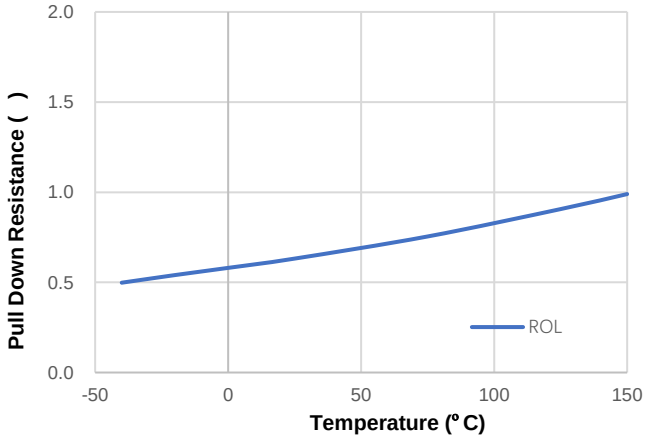


Figure 9. ROL vs Temperature

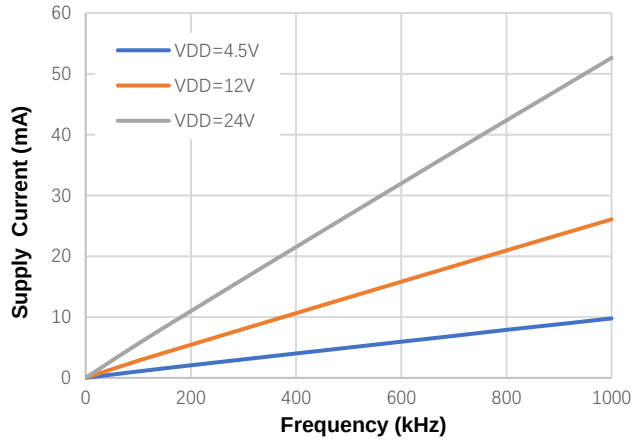
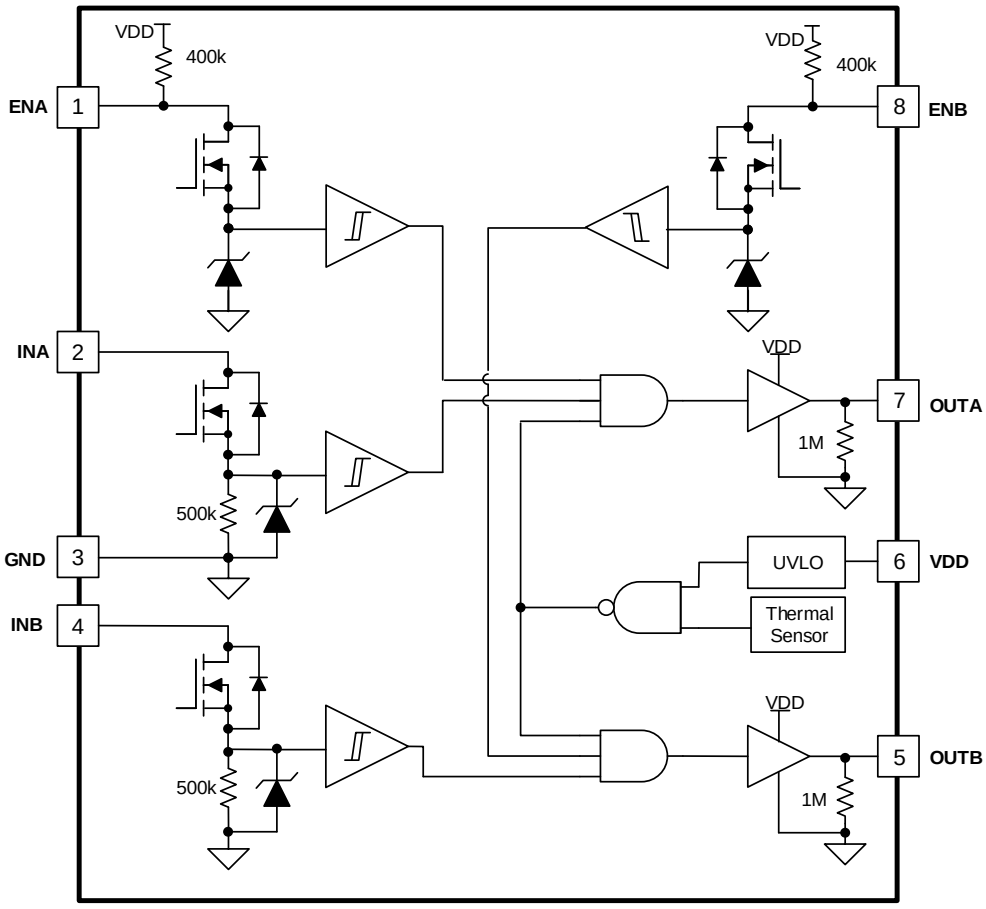


Figure 10. Operation Supply Current vs Frequency, C_{OUT}=1nF



Overview

The SCT52240Q is a dual-channel non-invertible high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with the minimum propagation delay 13ns from input to output. The 1ns delay matching and the stackable output characteristics support higher driving capability demanding in high power converter application. The ability to handle -5V DC input increases the noise immunity of driver input stage, the 24V rail-to-rail output improves the SCT52240Q output stage robustness during switching load fast transition. The SCT52240Q has flexible input and enable pin configuration, table 1 shows the device output logic truth table.

. Table 1: the SCT52240Q Device Logic.

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	Floating	Floating	L	L
Floating	Floating	L	L	L	L
Floating	Floating	L	H	L	H
Floating	Floating	H	L	H	L
Floating	Floating				

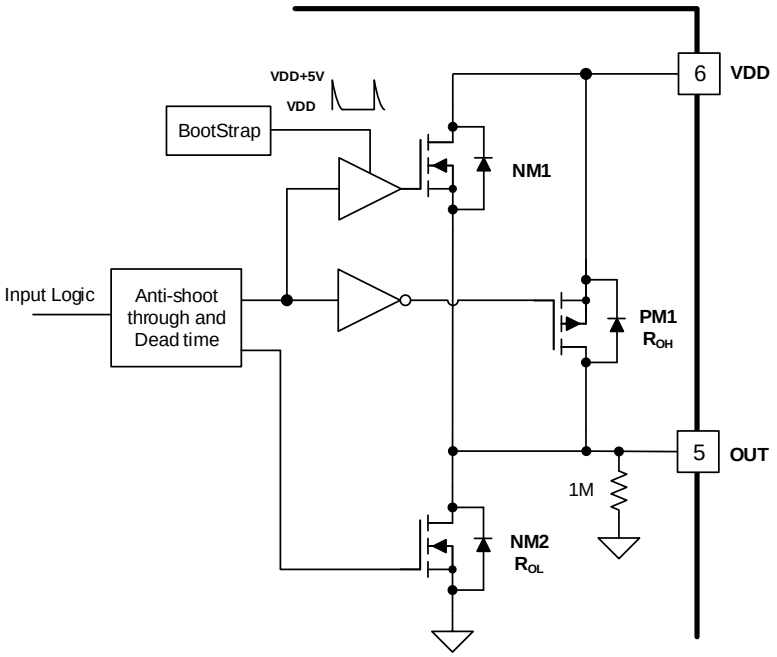


Figure 12. SCT52240Q Output Stage

Stackable Output

The SCT52240Q features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be stackable when the driven power device required higher driving capability. For example, in a Boost Power Factor Correction converter, there are 2 power MOSFET in parallel to support higher power output capability. The two power MOSFET are preferred to be driven by a common gate control signal. By using SCT52240Q, the OUTA and OUTB can be connected together to provide the higher driving capability, so does the INA and INB. As a result, a single input signal controls the stacked output combination. To support the stackable output, each channel output stage artificially implements up to 5ns dead-time to avoid the possible shoot-through between two channels as shown Figure 13.

Due to the rising and falling threshold mismatch between INA and INB, cautions must be taken when implementing stackable output of OUTA and OUTB together. The maximum mismatch between INA and INB input threshold is up to 10mV (maximum cross temperature), as a result the allowed minimum slew rate of input logic signal is 2V/us. The following suggestions are recommended when INA and INB connected together and along with the OUTA and OUTB:

1. Apply the fast slew rate dv/dt on input (2 V/us or greater) to avoid the possible shoot-through between OUTA and OUTB output stage.
2. INA and INB must be connected as close to the pins as possible.

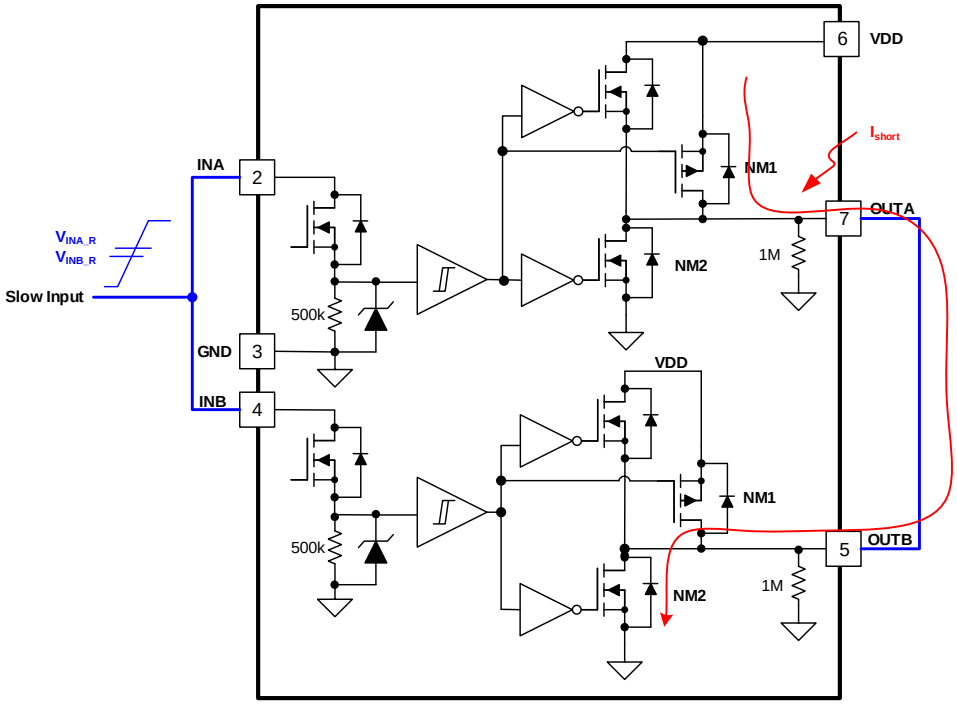


Figure 13. SCT52240Q Stackable output

The Figure 14 and Figure 15 shows the stackable output with 2V/us input signal.

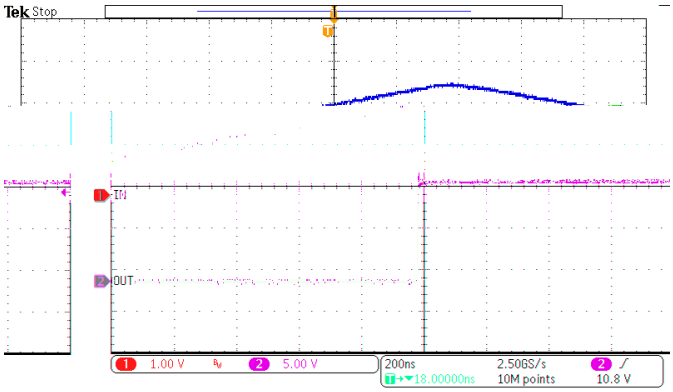


Figure 14. Driver Switching ON

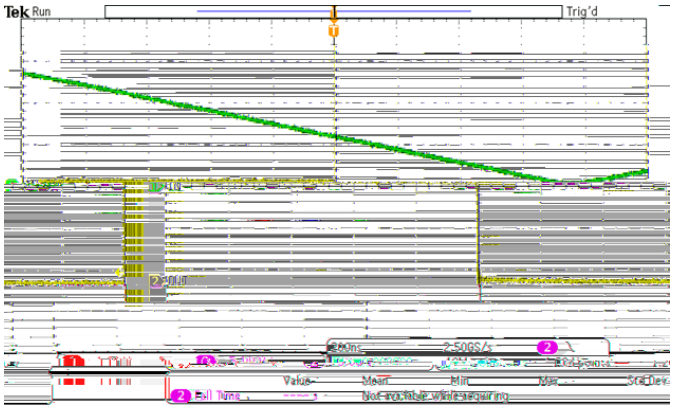


Figure 15. Driver Switching OFF

Thermal Shutdown

Once the junction temperature in the SCT52240Q exceeds 170° C, the thermal sensing circuit stops switching until the junction temperature falling below 145° C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

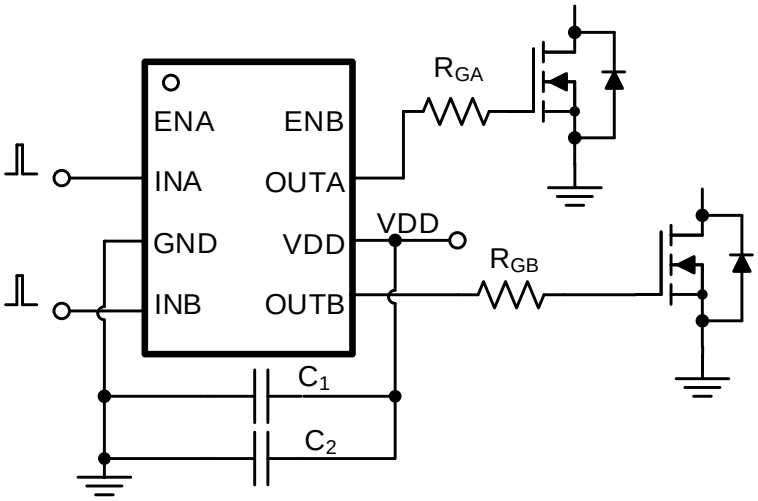


Figure 16. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52240Q depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52240Q features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52240Q is:

(1)

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- F_{SW} is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52240Q is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

(2)

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

$$ - \quad \left(\frac{\quad}{\quad} \quad \frac{\quad}{\quad} \right) \qquad (3) $$

Where

- R_{OH} is the equivalent pull up resistance of SCT52240Q
- R_{OL} is the pull down resistance of SCT52240Q
- R_G is the gate resistance between driver output and gate of power device.

Application Waveforms

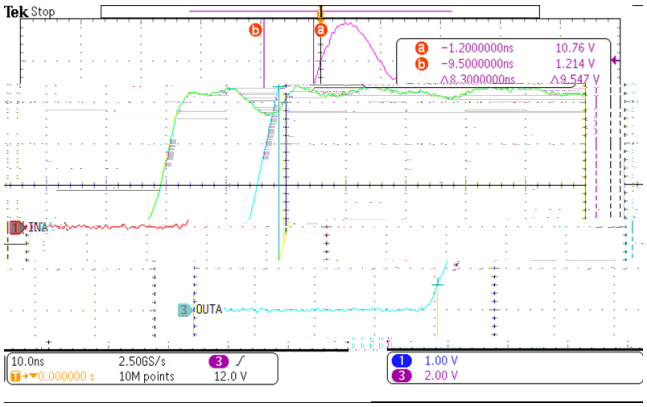


Figure 17. Driver Switching ON

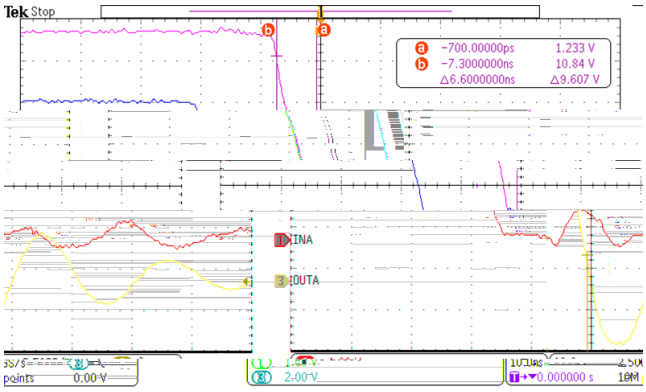


Figure 18. Driver Switching OFF

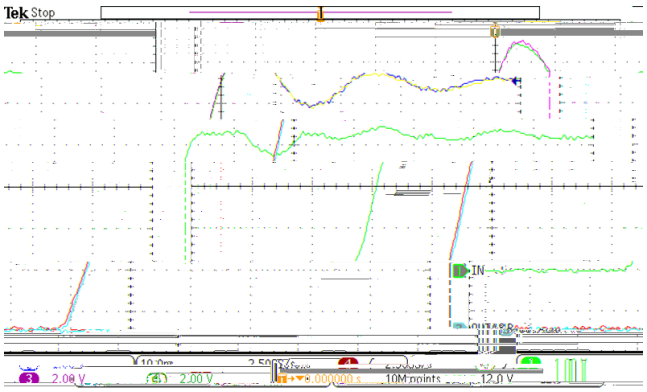


Figure 19. Delay Matching Rise

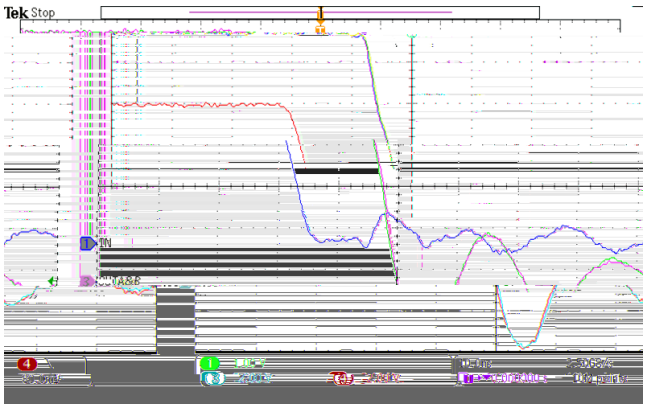


Figure 20. Delay Matching Fall

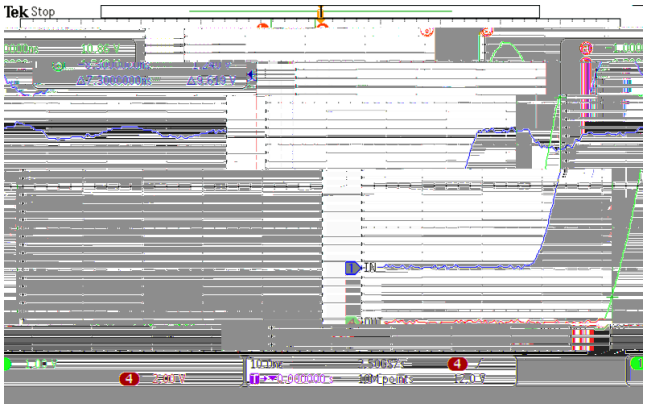


Figure 21. Stackable Output Rise

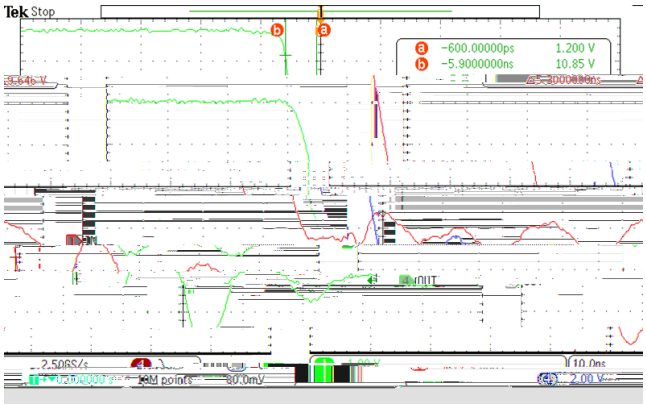


Figure 22. Stackable Output Fall

Layout Guideline

The SCT52240Q provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not designed well. The regulator could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. Below are the layout recommendations with using SCT52240Q and Figure 23 is the layout example.

Put the SCT52240Q as close as possible to the power device to minimize the gate driving loop including the driver output and power device gate. The power supply decoupling capacitors needs to be close to the VDD pin and GND pin to reduce the supply ripple. For the output stackable application, the driver input loop of two-channel input must be strictly symmetrical to ensure the input propagation delay is the same.

TOP VIEW

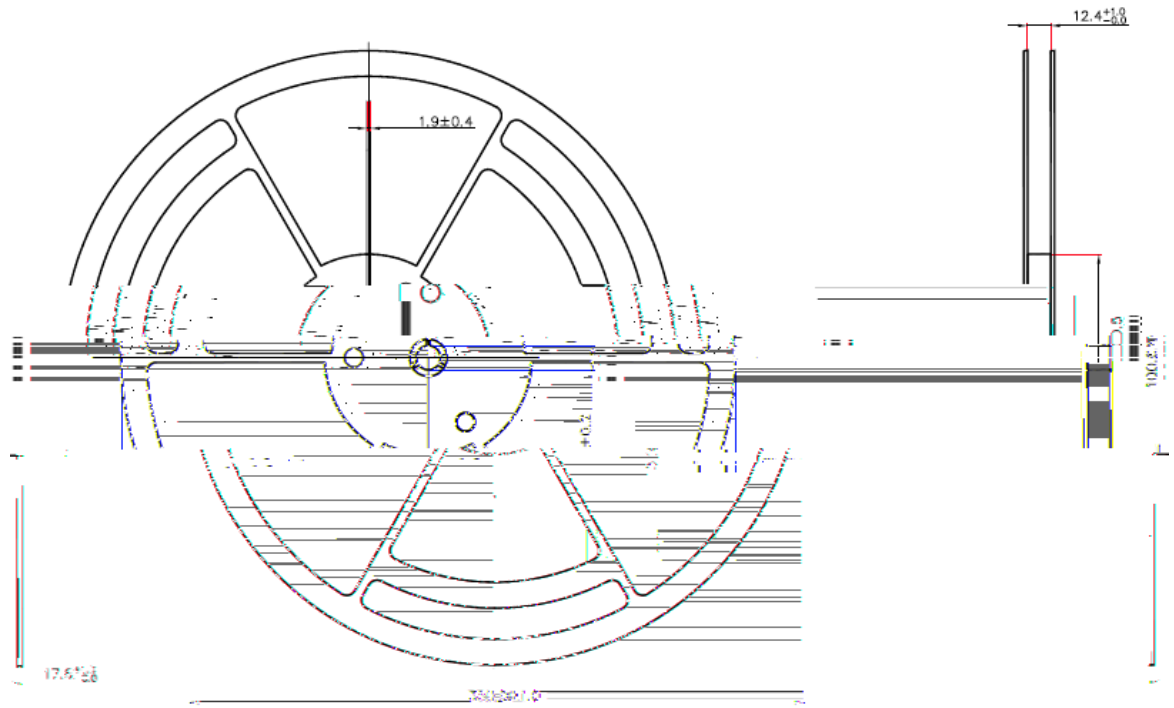
BOTTOM VIEW

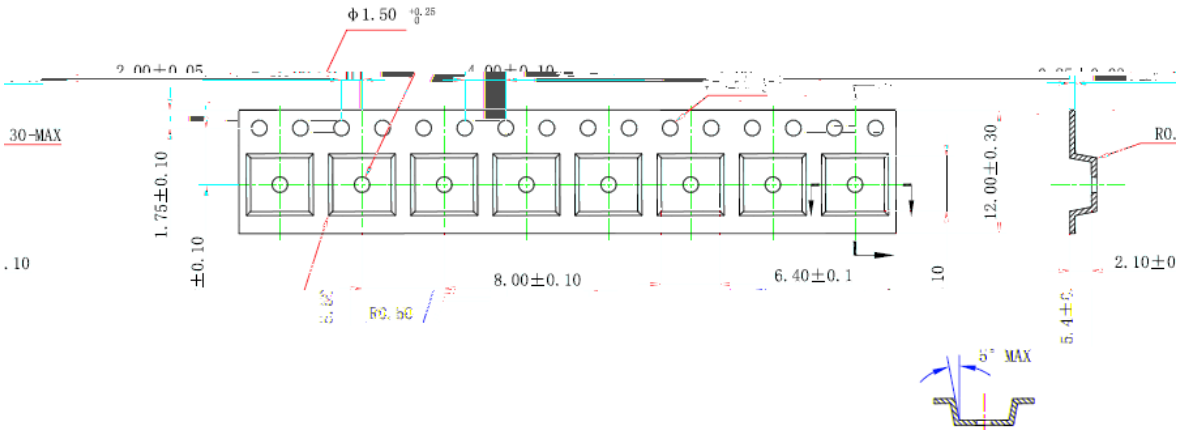
SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.

4.





Feeding Direction