OBSRPHLK EP LOV

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Customer sample

Revision 0.81: Update DEVICE ORDER INFORMATION

ABSF B LOABO KCLO HLK

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT63242FIBR	Tape & Reel	5000	3242	32	QFN-32L

PLIR B UF R OD HKDP

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	24	V
PVIN1, PVIN2	-0.3	22	V
SW1,SW2	-1	22	V
BST1,BST2	-0.3	26	V
BST1-SW1,BST2-SW2	-0.3	6	V
VDD, V3P3, VDM, EN, PWM1, PWM2, ISNS, IDMO, VDMO, QDET	-0.3	6	V
Operating junction temperature TJ(2)	-40	125	°C
Storage temperature TSTG	-65	150	°C

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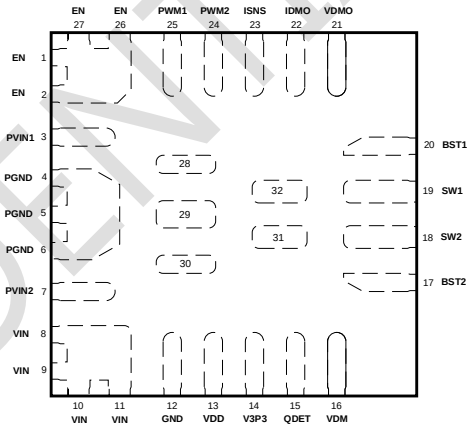

Figure 1. Top view 32-Lead QFN 4mm*4mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

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NAME	NO.	PIN FUNCTION
PVIN1	3,28	Input supply voltage of half-bridge FETs Q1 and Q2. Connected to the drain of high side FET Q1. a local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
PGND	4,5,6,29	PGND is the common power ground of the full bridge, connected to the source terminal of low side FETs Q2 and Q4 internally.
PVIN2	7,30	Input supply voltage of half-bridge FETs Q3 and Q4. Connected to the drain of high side FET Q1. Local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
VIN	8,9,10,11	Input supply voltage of the 5V LDO. Add a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
GND	12	Ground.

VDD	13	Output voltage of the 5V LDO. Connect 2.2uF capacitor from this pin to GND pin. VDD is also the input power supply for gate driver of power stage and the 3.3V LDO.
V3P3	14	3.3V LDO output. Connect 2.2uF capacitor to ground.
QDET	15	Q-factor detection input.
VDM	16	High-pass filter input. Voltage demodulation pin data packets based on coil voltage.
BST2	17	Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin.
SW2	18,31	Switching node of the half-bridge FETs Q3 and Q4.
SW1	19,32	Switching node of the half-bridge FETs Q1 and Q2.
BST1	20	Power supply bias for the high-side power MOSFET gate driver of Q1 as shown in the block diagram. Connect a 0.1uF capacitor from BST1 pin to SW1 pin.
VDMO	21	Voltage demodulation output.
IDMO	22	Current demodulation output.
ISNS	23	Current detection output. The voltage of the pin is proportional to the input current.
PWM2	24	PWM logic input to the FET Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q4, and turns on the high-side FET Q3. Logic LOW turns off the high-side FET Q3 and turns on the low-side FET Q4. When PWM input is in the tri-state mode, both Q3 and Q4 are turned off.
PWM1	25	PWM logic input to the FET Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q2, and turns on the high-side FET Q1. Logic LOW turns off the high-side FET Q1 and turns on the low-side FET Q2. When PWM input is in the tri-state mode, both Q1 and Q2 are turned off.

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63242 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63242. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

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V_{PVIN1}=V_{PVIN2}=12V, VDD=5V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supplies and UVLO						
V_{IN}	Operating input voltage		4.2		20	V
P_{VIN}	Operating input voltage		1		20	V
V_{IN_UVLO}	V_{IN} UVLO Threshold Hysteresis	V_{IN} rising		3.45 370		V mV
V_{DD_UVLO}	V_{DD} UVLO Threshold Hysteresis	V_{DD} rising		3.7 440		V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0V, VIN=12V		2	3	A
I_{SHDN_PVIN}	Shutdown current from PVIN1,PVIN2	EN=0V, PVIN=12V		1	3	uA
I_{VINQ}	[redacted]	EN floating, no loading on LDO		630		uA
[redacted]	Quiescent current from PVIN1, PVIN2	EN floating, no loading on LDO		50		uA
ENABLE INPUTS and PWM logic						
V_{EN_H}						

V_{ISNS2}	Voltage with 1A input current	I_{PVIN}=1A, Tj=25	1.568	1.6	1.632	V
Protection						
T_{SD}	Thermal shutdown threshold Hysteresis	T_J rising		155 35		°C °C

Figure 2. Transfer Efficiency with 5W RX@ Vout=5V

Figure 3. Transfer Efficiency with 10W RX@ Vout=9V

Figure 4. Transfer Efficiency with 15W RX@ Vout=12V

Figure 5. 5V LDO Iout vs Vout

Figure 6. 3.3V LDO Iout vs Vout

Figure 7. Current S[S)864 Tm4MCID 40/Lang (en-US)

3.3V LDO

The SCT63242 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Q Factor Detection

The SCT63242 integrated a low cost, reliable Q factor detection circuit to assure foreign objects detection before the selection phase. It generates a small pulse to detect any foreign object on the transmitter coil, it can detect metal on the transmitter coil easily.

After chip enable, apply a low voltage level pulse to EN pin can trigger the Q factor detection feature. The pulse width should be longer than 50us but less than 200us. SW1 will be preset to 2V for 4.7ms and then pull low to ground and this apply power to LC resonant loop and Vcoil will appear damping oscillation after SW1 short to ground. The SCT63242 will generate a pulse on VDMO pin and MCU can capture this pulse to calculate the Q factor by the pulse width as the Equation 4 shows. PWM1 and PWM2 should be low in Q factor detection phase.

(4)

where

- T is the pulse width on VDMOS pin
- V_{TH_HIGH} is high threshold 0.2V
- V_{TH_LOW} is low threshold 0.1V

Voltage and Current Demodulation

The SCT63242 integrates two demodulation schemes, one based on coil voltage information calling voltage demodulation and the other based on input average current information calling current demodulation.

The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure10. This simple implementation achieves the envelope detector function, low-pass filter as well as the DC filter function. The envelope detector applies the analog signal to VDM pin and the chip do the demodulation and output a digital signal to VDMO pin which MCU can capture the voltage demodulation results and then implement the packet decode.

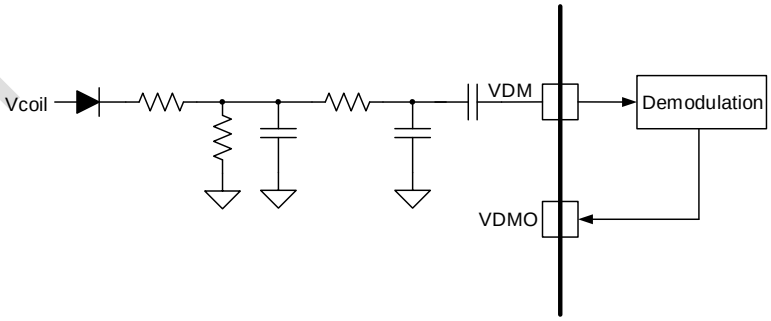

Figure 10. Envelope Detector

The current-mode detector takes the modulation information from the average input current which the chip can read from ISNS pin. The MCU can detect the demodulation results on VDMO and IDMO pins and then implement the packet decode.

Thermal Shutdown

The SCT63242 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 155C, the thermal sensing circuit stops two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 120C, then the device restarts.

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Typical Application

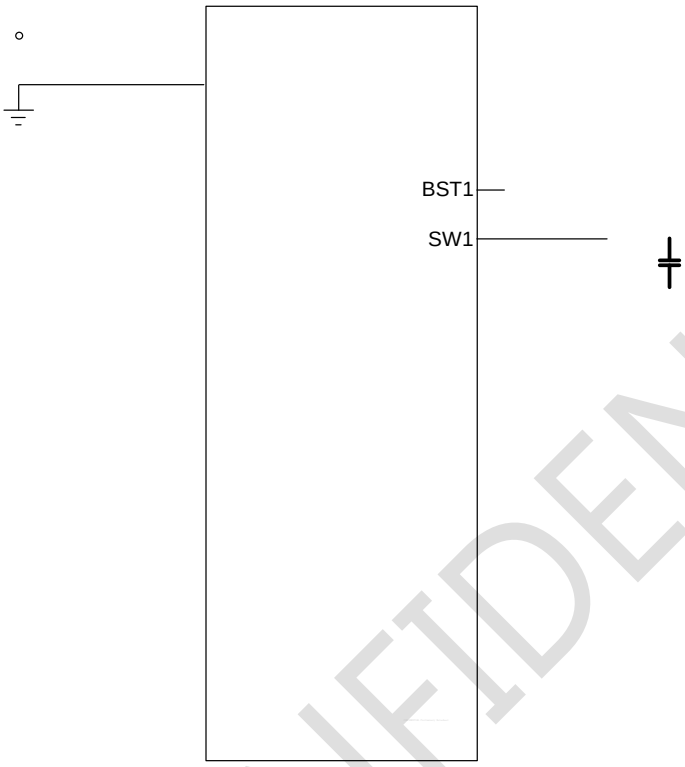

Figure 11. Same Input to VIN and PVIN

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Application Waveforms

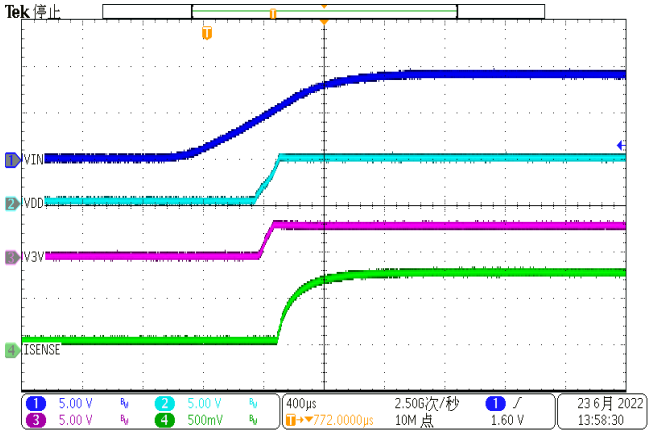


Figure 12. Power Up

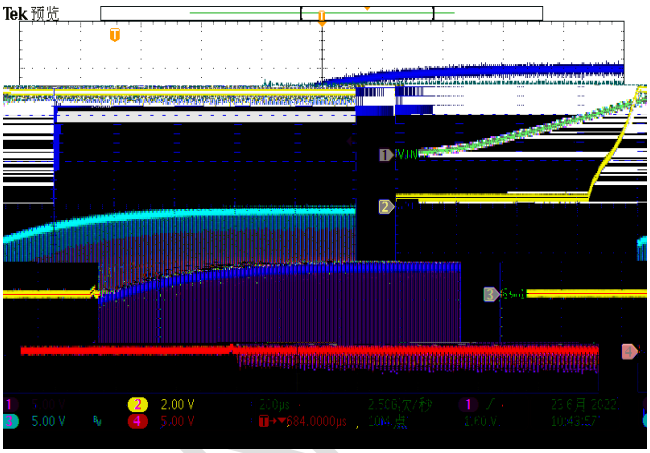


Figure 13. Power Up

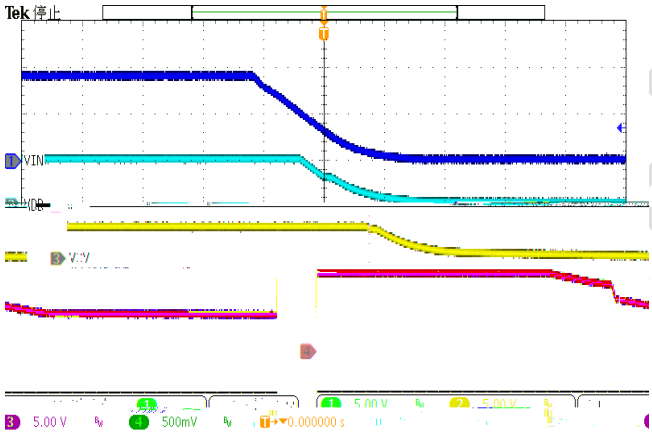


Figure 14. Power Down

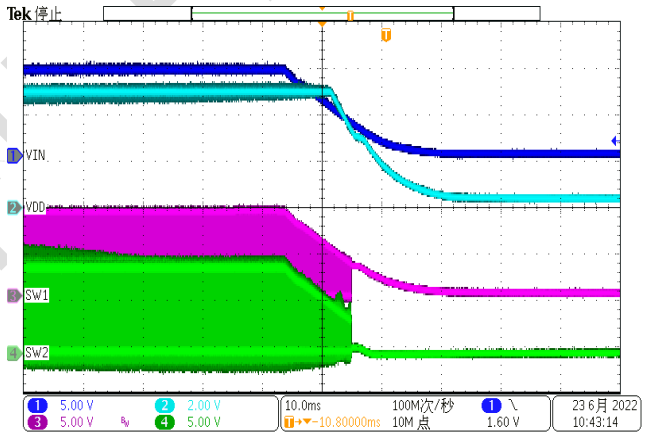


Figure 15. Power Down

Figure 16. Full bridge @Vin=9V, RX=10W

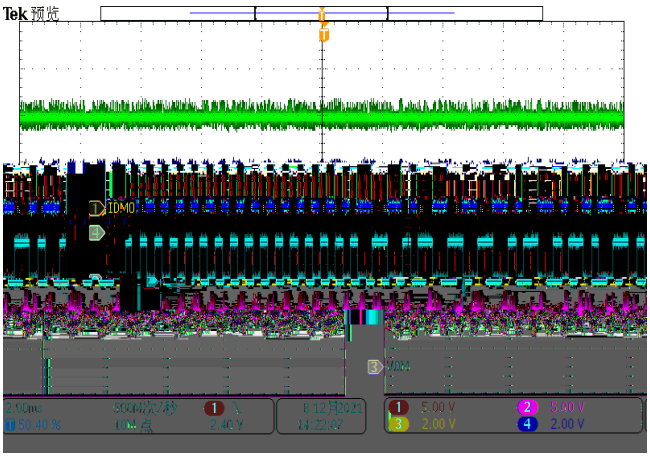


Figure 17. VDMO IDMO Demodulation Output

Layout Guideline

Proper PCB layout is a critical for SCT63242 For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Bypass capacitor for VDD place next to VDD pin.
5. Bypass capacitor for V3V place next to V3V pin.

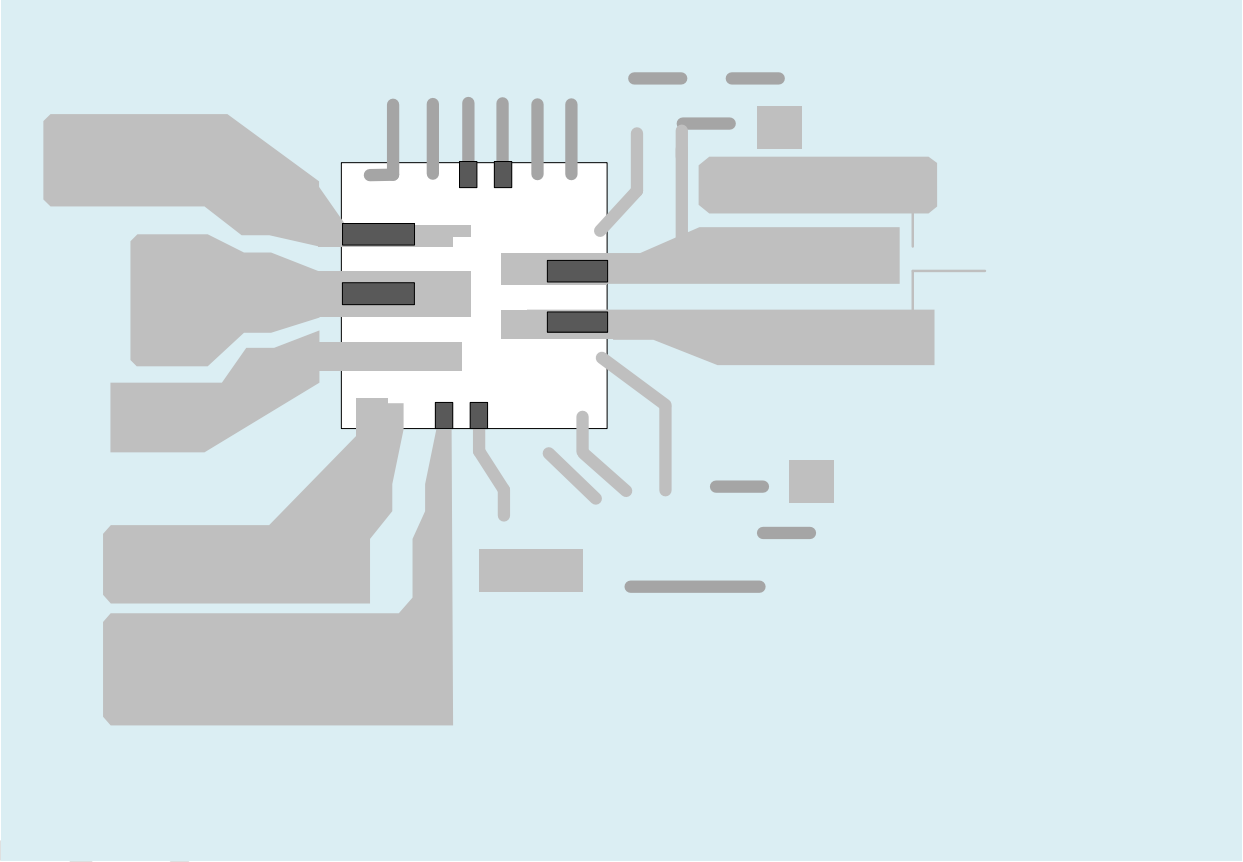
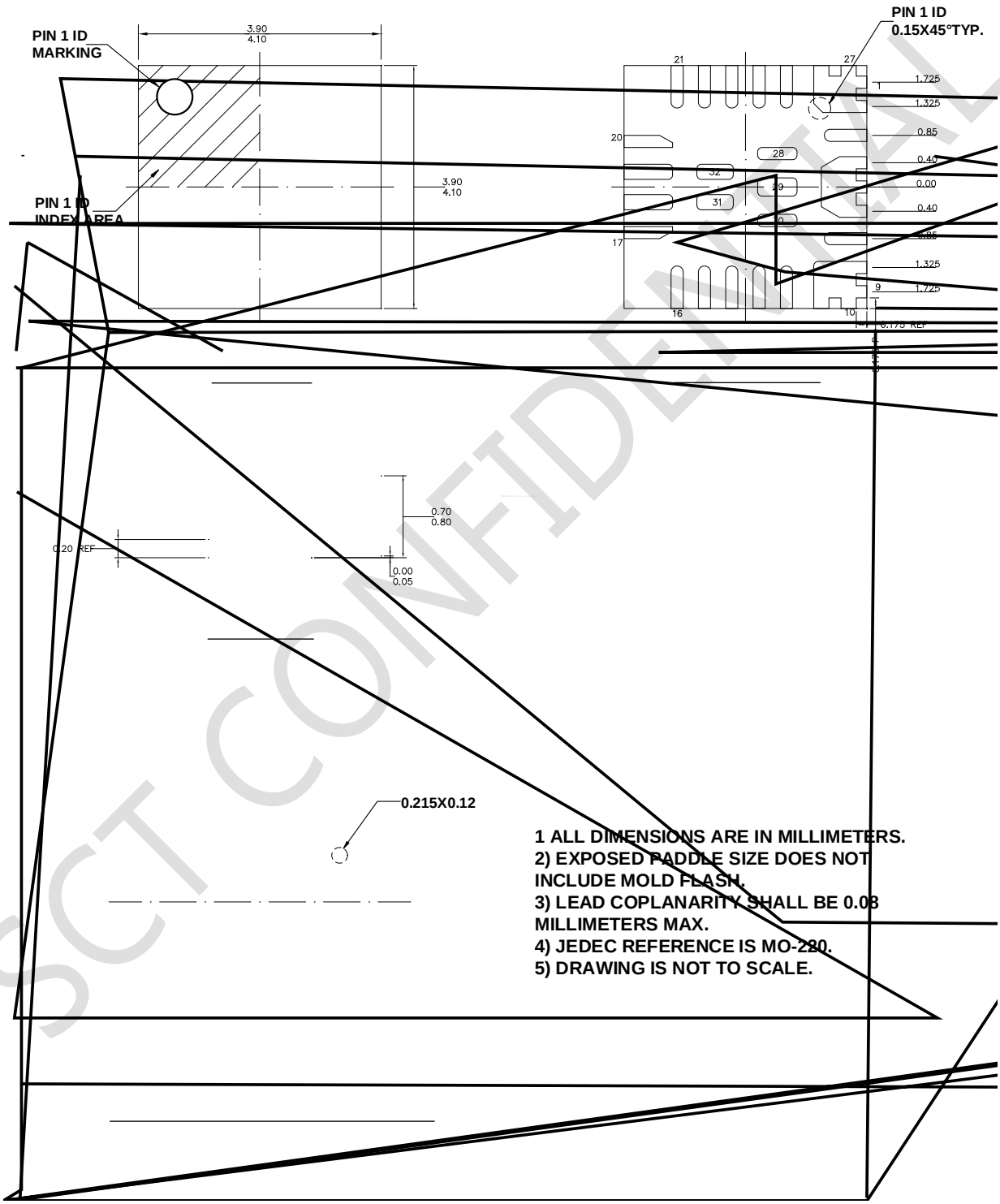


Figure 18. PCB Layout Example

M H DB KCL O FL K

QFN -32L (4mm x 4mm)



MB KA OBBI RKCL O RL K