- Wide Supply Voltage Range: 4.5V - 24V
- 4A Peak Source Current and 4A Peak Sink Current
- Dual Input Configuration: Non-Inverting (IN+) or Inverting (IN-) Input
- Negative Input Voltage Capability: Down to -5V
- TTL Input-Logic Threshold
- Propagation Delay: 12ns
- Fast Rising and Falling Time: 8ns and 6ns
- Low Quiescent Current: 28uA
- Under Voltage Lock Out Protection of Supply Voltage
- Output Low When Input Floating
- Thermal Shutdown Protection: 175°C
- Available in TSOT23-5L Package

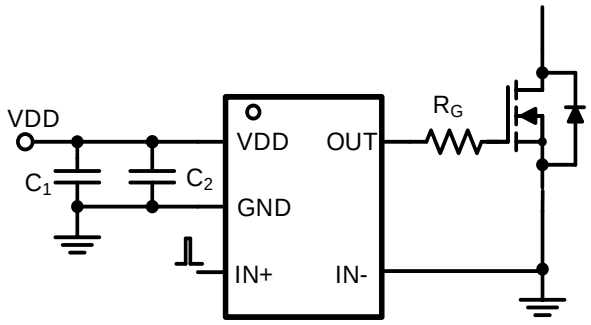
- Power MOSFET Gate Driver
- IGBT Gate Driver
- GaN Device Gate Driver
- Switching Power Supply
- Motor Control, Solar Power

The SCT51240A is a wide supply, single channel, high speed, low side gate driver for power MOSFET, IGBT, and wide band-gap device such as GaN. The 24V power supply rail enhances the driver output ringing endurance during the power device transition. The capability to switch below 5V power supply makes the SCT51240A work well for the low voltage threshold power device.

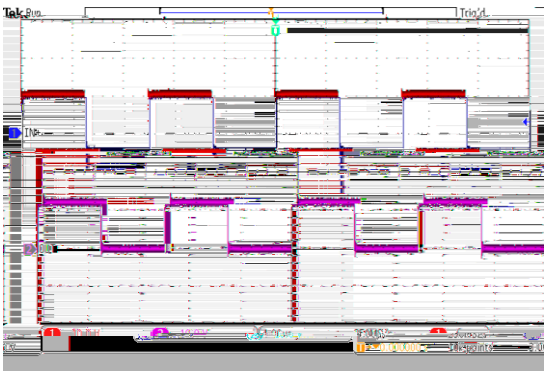
The SCT51240A can source and sink 4A peak current along with rail-to-rail output driving capability. The minimum 12ns input to output propagation delay enables it suitable for high frequency power converter application. The SCT51240A features wide input hysteresis that is compatible for TTL low voltage logic. The SCT51240A has the capability to handle negative input down to -5V, which enhances the input noise immunity. The IN+ and IN- input provides the flexibility to configure the SCT51240A either as non-inverting or inverting driver.

The SCT51240A has very low quiescent current that reduces the standby power loss in the power converter. The SCT51240A gate driver adopts non-overlap driver design to avoid the shoot-through of output stage.

The SCT51240A features 175°C thermal shut down protection and operates over a wide temperature range -40°C to 150°C. The SCT51240A is available in TSOT23-5L package.



SCT51240A Typical Application



Application Waveform

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Over operating free-air temperature range unless otherwise noted

PARAMETER

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V_{DD}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{DD}	Operating supply voltage		4.5		24	V
V_{DD_UVLO}	Input UVLO Hysteresis	V_{DD} rising		4.2 300	4.48	V mV
I_Q	Quiescent current	IN+=IN-=GND or IN+=IN-=VDD, VDD=3.5V		28	65	uA
		IN+=IN-=GND, V_{DD}=12V		110	190	uA
INPUTS						
V_{IN+}	Input+ logic high threshold			2.15		V
V_{IN+}	Input+ logic low threshold			1.15		V
V_{IN+_Hys}	Hysteresis			1		V
V_{IN-_H}	Input- logic high threshold			2.15		V
V_{IN-_L}	Input- logic low threshold			1.1		V
V_{IN-_Hys}	Hysteresis			1.05		V
OUTPUTS						
$V_{DD}\_V_{OH}$	Output High Voltage (only PMOS ON)	I_{OUT}=10mA		50	100	mV
V_{OL}	Output Low Voltage	I_{OUT}=10mA		5	10	mV
$I_{SINK/SRC}$	Output Sink/Source peak current	C_{Load}=10nF, F_{sw}=1kHz		4		A
R_{OH}	Output pull high resistance (only PMOS ON)	I_{OUT}= -10mA		5	10	
R_{OL}	Output pull low resistance	I_{OUT}= 10mA		0.5	1	
Timing						
T_R	Output rising time	C_{Load}=1nF		9		ns
T_F	Output falling time	C_{Load}=1nF		6		ns
T_{D_IN+}	IN+ to output propagation delay, Rising edge			12		ns
	IN+ to output propagation delay, Falling edge			12		ns
T_{D_IN-}	IN- to output propagation delay, Rising			12		ns
	IN- to output propagation delay, Falling			12		ns
T_{MIN_ON}	Minimum input pulse width	C_{Load}=1nF		20		ns
Protection						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
	Hysteresis			30		°C

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V_{DD}=12V, T_A= 25°C.

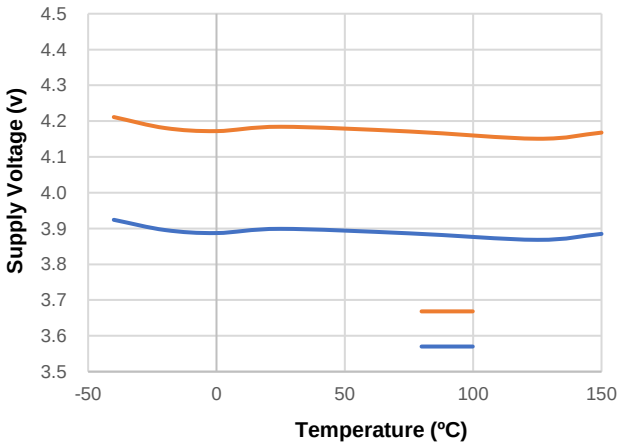

Figure 1. UVLO Vs Temperature

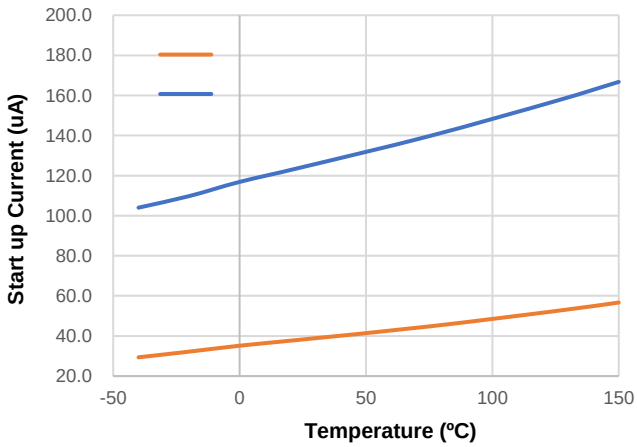

Figure 2. Start-up current Vs Temperature

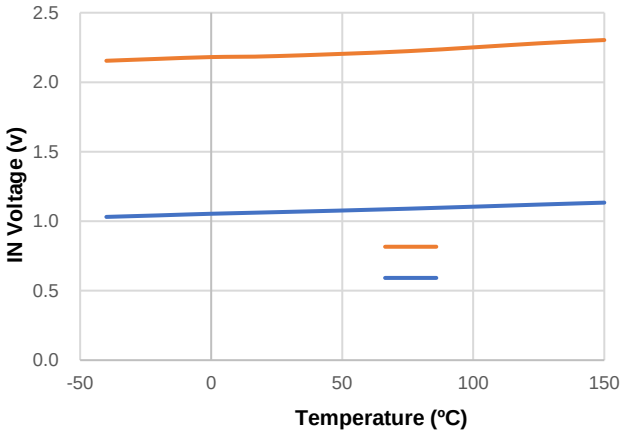

Figure 3. IN Threshold Vs Temperature

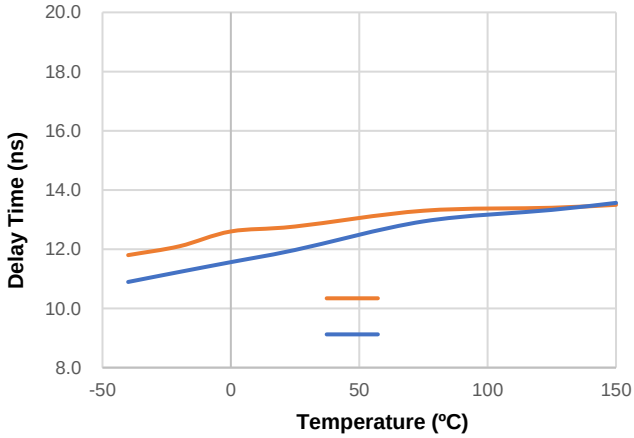

Figure 4. Input to Output Propagation Delay vs Temperature

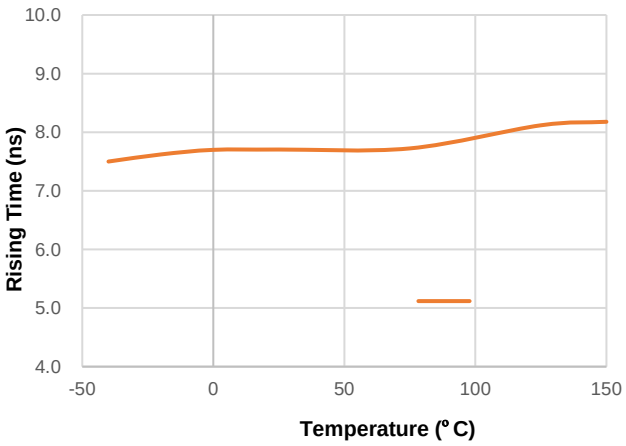

Figure 5. Output Rising Time Vs Temperature

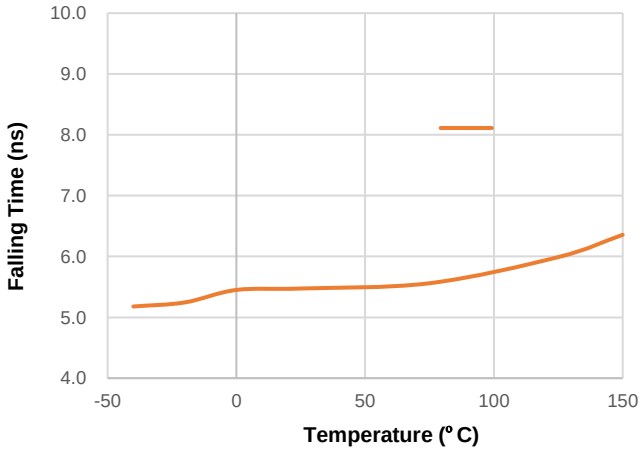

Figure 6. Output Falling Time Vs Temperature

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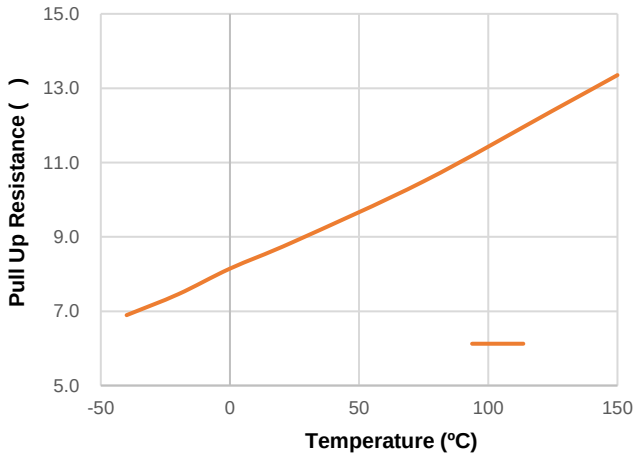

Figure 7. ROH vs Temperature

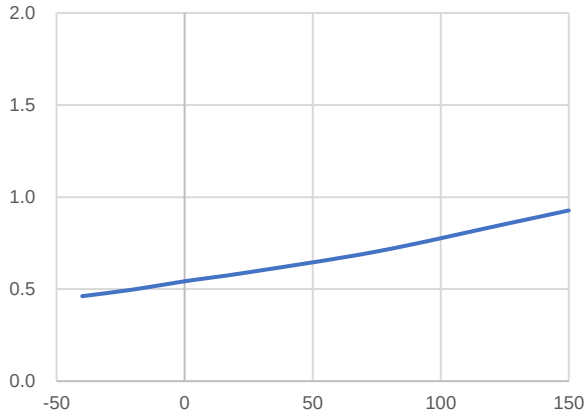

Figure 8. ROL Vs Temperature

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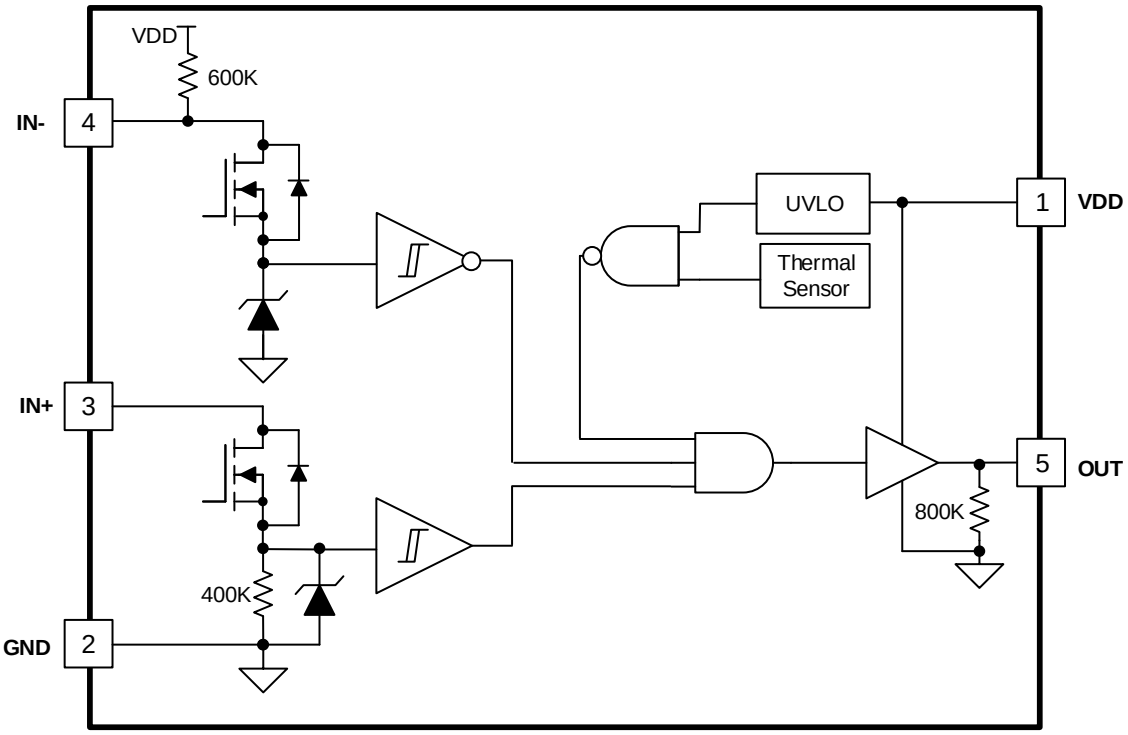

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Overview

The SCT51240A is a up to 24V wide supply, single channel, high speed, low side gate driver for power MOSFET and IGBT. The SCT51240A can source and sink 4A peak current along with the minimum propagation delay 12ns from input to output. The ability to handle -5V DC input increases the driver input stage noise immunity, the 24V rail-to-rail output improves the SCT51240A output stage robustness during the switching load fast transition.

The SCT51240A features a dual-input design by implementing both inverting (IN pin) and non-inverting (IN+ pin) configuration in the same device. Either the IN+ or IN pin can be used to control the state of the driver output. The internal pull-up or pull-down resistors on the input pins ensure that output is held low when the input pins are in floating condition. As a result, the unused input pin must be biased properly to ensure that driver output is enabled for normal operation. Table 1 is the device logic truth table.

Table 1: the SCT51240A Device Logic.

IN+	IN-	OUT
L	L	L
L	H	L
H	L	H
H	H	L
Floating	Any	L
Any	Floating	L

VDD Power Supply

The SCT51240A operates under a supply voltage range between 4.5V to 24V. For the best high-speed circuit performance, two VDD bypass capacitors in parallel are recommended to prevent noise problems on supply VDD. A 0.1- F surface mount ceramic capacitor must be located as close as possible to the VDD to GND pins of the SCT51240A. In addition, a larger capacitor (such as 1 F or 10uF) with relatively low ESR must be connected in parallel, in order to help avoid the unexpected VDD supply glitch. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

Under Voltage Lock Out (UVLO)

The SCT51240A Under Voltage Lock Out (UVLO) rising threshold is typically 4.2 V with 300-mV typical hysteresis. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low regardless of the status of the inputs. The hysteresis prevents output bouncing when low VDD supply voltages have noise impact from the power supply. The capability to operate at low power supply voltage below 5 V is especially suited for driving wide band gap power device like GaN. For example, during power up, the driver output remains low until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with VDD till steady state VDD reached.

The non-inverting operation in Figure 9 shows that the output remains low till the UVLO threshold reached, and then the output is in-phase with the input.

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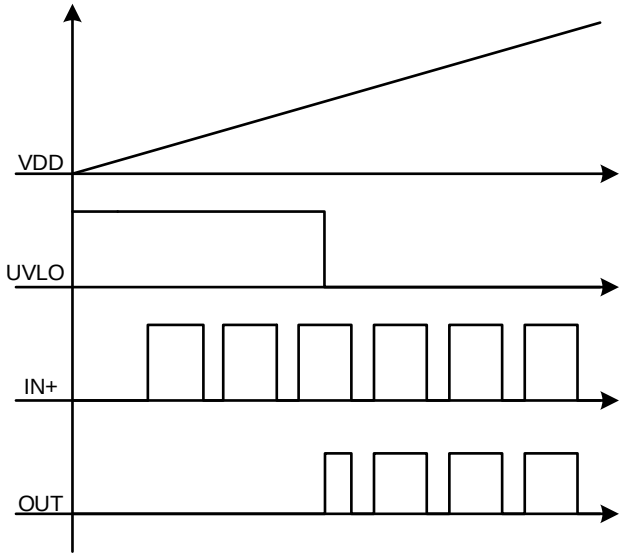

Figure 9. SCT51240A Output Vs VDD

Input Stage

The input of SCT51240A is compatible on TTL logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1.0 V, the logic level thresholds are conveniently driven by PWM control signals derived from 3.3 V and 5.9 V digital power controller devices. Wider hysteresis offers enhanced noise immunity compared to the traditional TTL logic implementation, where the hysteresis is typically less than 0.5 V. SCT51240A also features tight control of the input threshold voltage that ensures stable operation across temperature. The low input capacitance on the input pins increases switching speed and reduces the propagation delay.

The SCT51240A features a dual-input configuration with two input pins available to control the gate voltage

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path to damp overshoots and undershoots. The outputs of the dual channel drivers are designed to withstand 500-mA reverse current without either damaging the device or causing the logic malfunction.

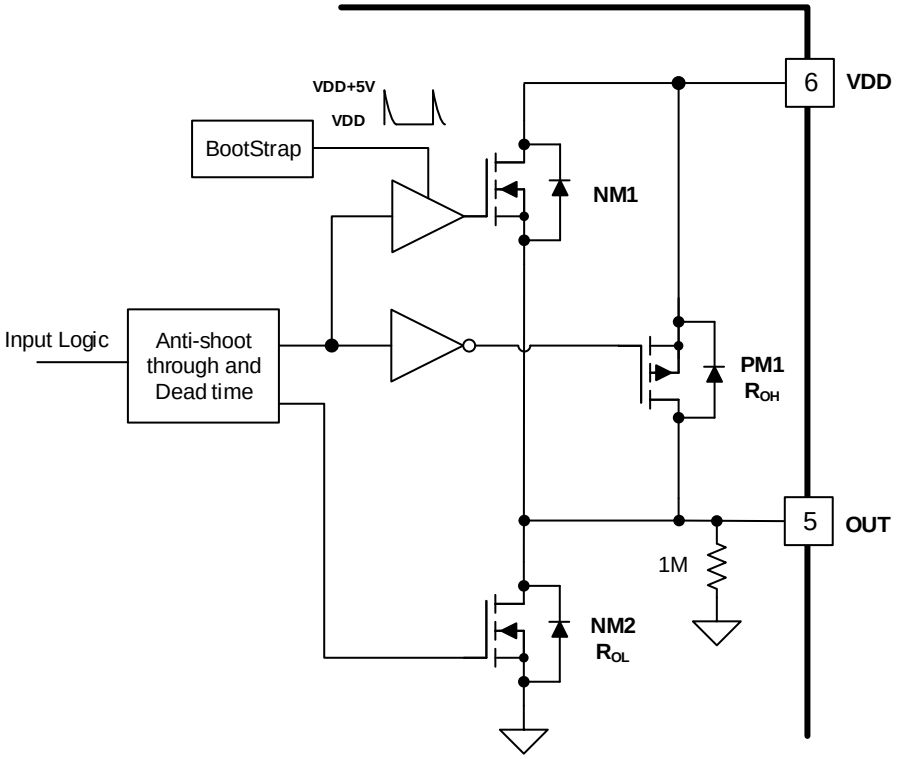

Figure 10. SCT51240A Output Stage

Thermal Shutdown

Once the junction temperature in the SCT51240A exceeds 175° C, the thermal sensing circuit stops switching until the junction temperature falling below 145° C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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Typical Application

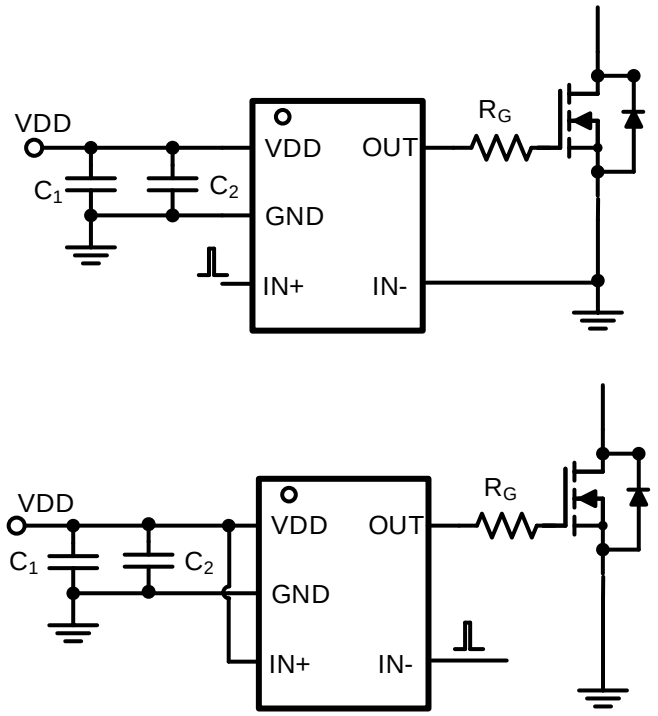

Figure 11. Single Channel Driver Non-Inverting and Inverting Application

Driver Power Dissipation

Generally, the power dissipated in the SCT51240A depends on the gate charge required of the power device (Qg), Switching frequency, and use of external gate resistors. The SCT51240A features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of SCT51240A is:

(1)

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- f_{SW} is the switching frequency

For the switching load of power MOSFET, the power loss of the driver is shown in equation (1), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effect of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications with the typical and maximum gate charge, in nC, to switch the device under specified conditions.

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(2)

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

(3)

Where

- R_{OH} is the equivalent pull up resistance of SCT51240A
- R_{OL} is the pull down resistance of SCT51240A
- R_G is the gate resistance between driver output and gate of power device.

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Application Waveforms

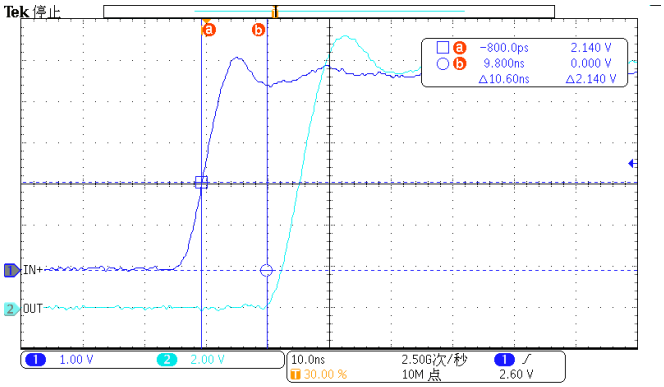

Figure 12. IN+ Switching ON(T_{DR})

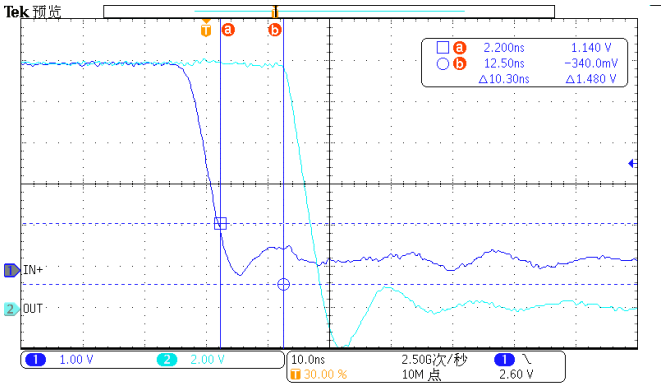

Figure 13. IN+ Switching OFF(T_{DF})

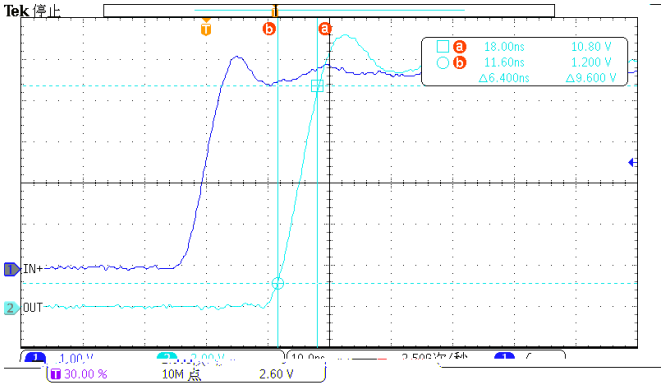

Figure 14. IN+ Switching ON(T_R)

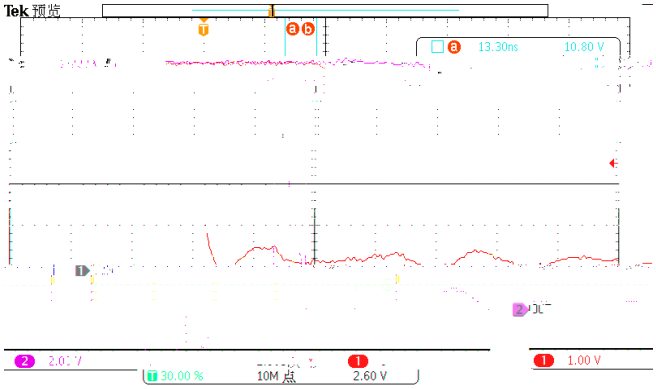

Figure 15. IN+ Switching OFF(T_F)

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Application Waveforms

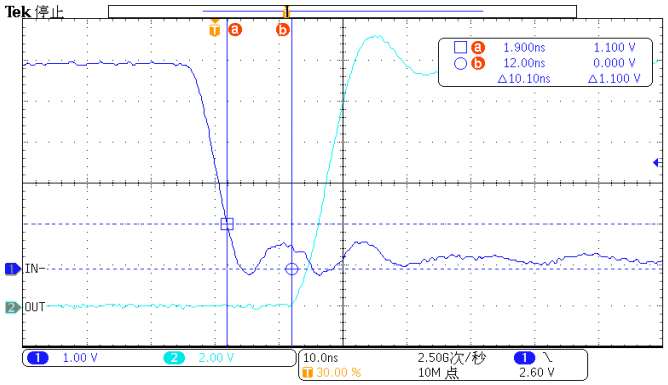

Figure 16. IN- Switching ON(T_{DR})

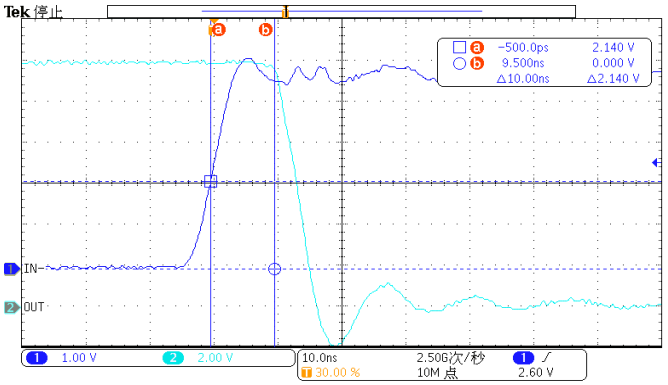

Figure 17. IN- Switching OFF(T_{DF})

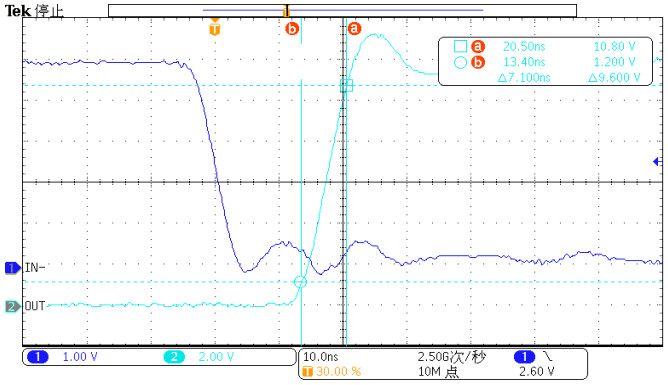

Figure 18. IN- Switching ON(T_R)

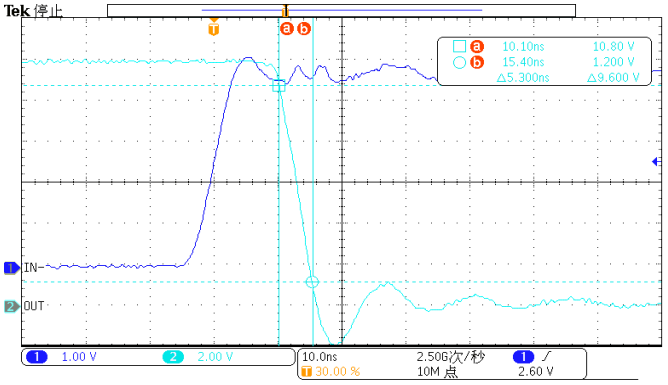

Figure 19. IN- Switching OFF(T_F)

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Layout Guideline

The SCT51240A provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not optimized. The regulator could suffer from malfunction and EMI noise if the power device gate has serious ringing. Below are the layout recommendations with using SCT51240A and Figure 16 is the layout example.

Put the SCT51240A as close as possible to the power device and minimize the gate driving loop including the driver output and power device gate. The power supply decoupling capacitors needs to be close to the VDD pin and GND pin to reduce the supply ripple.

Star-point grounding is recommended to minimize noise coupling from one current loop to the other. The GND of the driver connects to the other circuit node such as source of power MOSFET or ground of PWM controller at single point. The connected paths must be as short as possible to reduce parasitic inductance. A ground plane provides noise shielding and thermal dissipation as well.

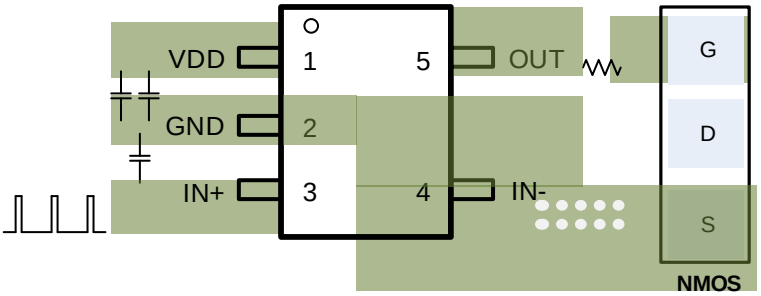

Figure 20. SCT51240A PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 170°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (4).

(4)

where

- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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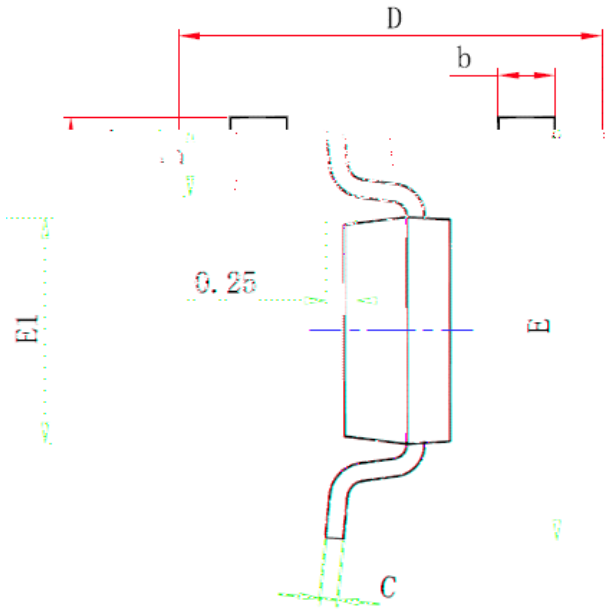
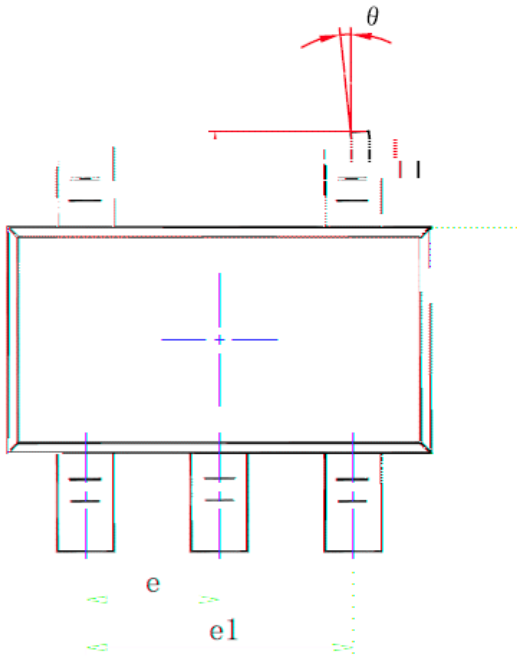
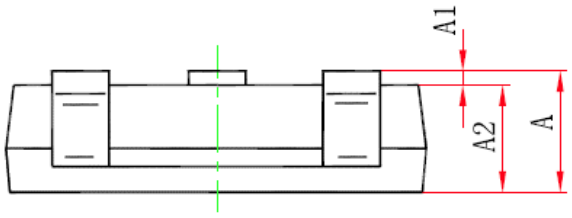


TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	---	---	0.9
A1	0.02	---	0.09
A2	0.7	---	0.8
b	0.35	---	0.5
c	0.08	---	0.2
D	2.82		3.02
E	2.65		2.95
E1	1.6		1.7
e	0.95 (BSC)		
e1	1.90 (BSC)		
L	0.3		0.6
	0°		8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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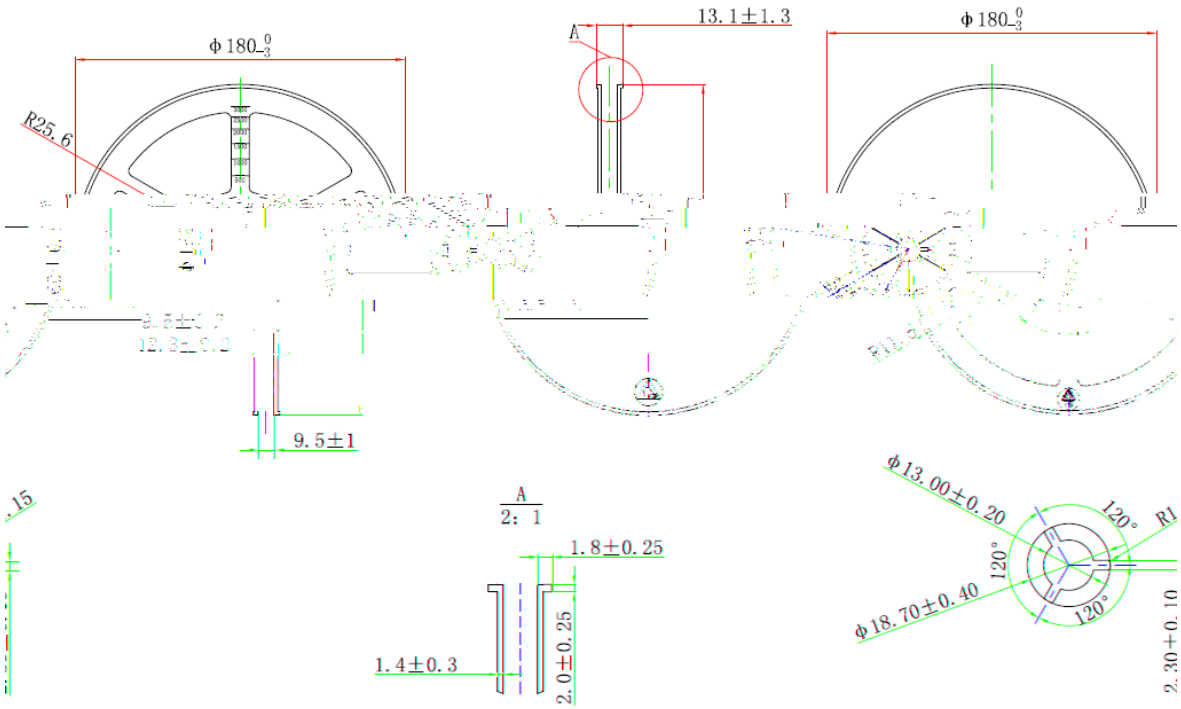

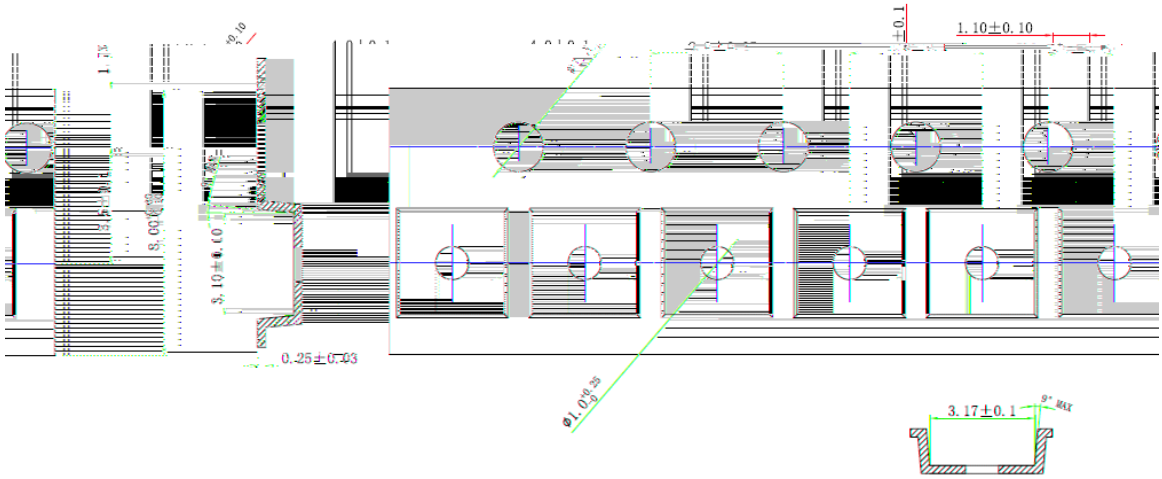

Feeding Direction

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