19V Vin Quad Channel Power Management IC for Safety Applications

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide Input Voltage Range: 3.5-19V
- Three High-Efficiency Step-Down Converters:
  - HV Buck1: Vout1=2.7-5V with 100mV Steps, Up to 2A Continuous Output Current
  - LV Buck2/3: Vout2/3=0.6-2.15V with 50mV Steps, Up to 2A Continuous Output Current
- One Low-Dropout Regulator (LDO):
  - LDO4: Vout4=1.6-3.5V with 50mV Steps, Up to 300mA Continuous Output Current
  - High PSRR: 60dB@10kHz, 60dB@100kHz, 40dB@1MHz
  - Low noise: 30 V rms total integrated noise from 100Hz to 100kHz
- ±1.5% Output Voltage Accuracy
- 2.2MHz Fixed Switching Frequency
- Integrated Frequency Dither for EMI Mitigation
- Selectable Light-load Operation: FCCM/PSM
- Programmable Power Sequencer
- Selectable RESETB Output: Open-drain/Push-pull
- Two GPIOs for Flexible System Management
- Integrated Protection Features:
  - Output Over-voltage/Under-voltage Protection
  - Over Current Protection
  - Input Under-voltage Lockout
  - Input Over-voltage Protection
  - Thermal Shutdown Protection: 175°C
- Functional Safety Features:
  - Compliance with ISO26262 Development
  - Hardware Integrity to Support ASIL-C System
  - ASIL-C Device Certification
  - QA & Simple Watchdog
  - Built-in Self Test (BIST)
- Up to 1MHz I2C Interface with Optional Packet Error Checking (PEC)
- Available in QFN-20L(2.5mm×3.5mm) Package with Wettable Flanks

DESCRIPTION

The SCT61242S is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high-efficiency synchronous buck converters (HV Buck1, LV Buck2 and LV Buck3) and one high-PSRR, low noise LDO (LDO4) with OV/UV monitoring and flexible power sequence for all outputs.

Buck1 has an input voltage range from 3.5 to 19V for connections to Power over Coax (PoC). Buck2 and Buck3 are identical and powered from the output of Buck1. All three buck converters can operate in either FCCM or PSM mode at light load, with 2.2MHz switching frequency and optional Frequency Spread Spectrum (FSS) function for EMI mitigation. LDO4 is a high PSRR, low noise LDO designed for analog power rail with a continuous output current of up to 300mA. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution.

The SCT61242S is featured with two configurable GPIO pins for flexible system management. For instance, GPIO1 could be configured as external voltage monitor input while GPIO2 configured as external regulator enable output to monitor and control an external power rail.

The SCT61242S integrated protection features including input under-voltage protection, input over-voltage protection, output over-voltage/under-voltage protection, over-current protection and thermal shutdown at 175°C.

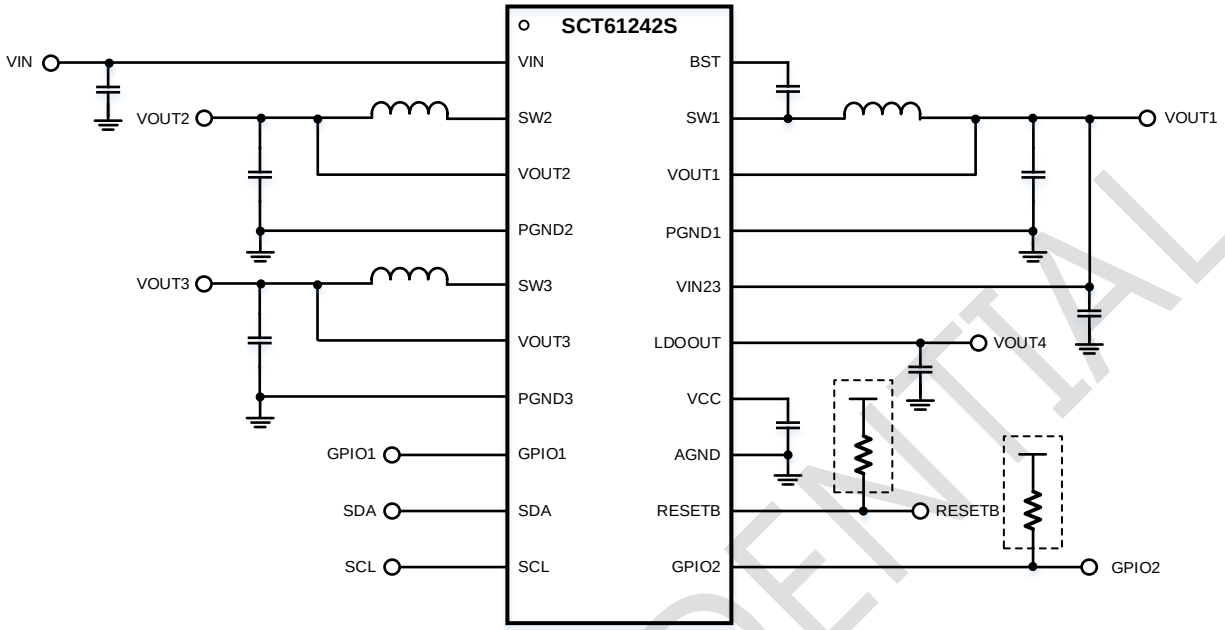
The SCT61242S provides Built-in Self Test (BIST) diagnosis over internal analog and digital circuits. All critical comparator and data will be checked at power-up stage. Watchdog is also supported to further improve system safety. The watchdog could be fed by periodic trigger pulse or specific I2C write operation with programmable timing window.

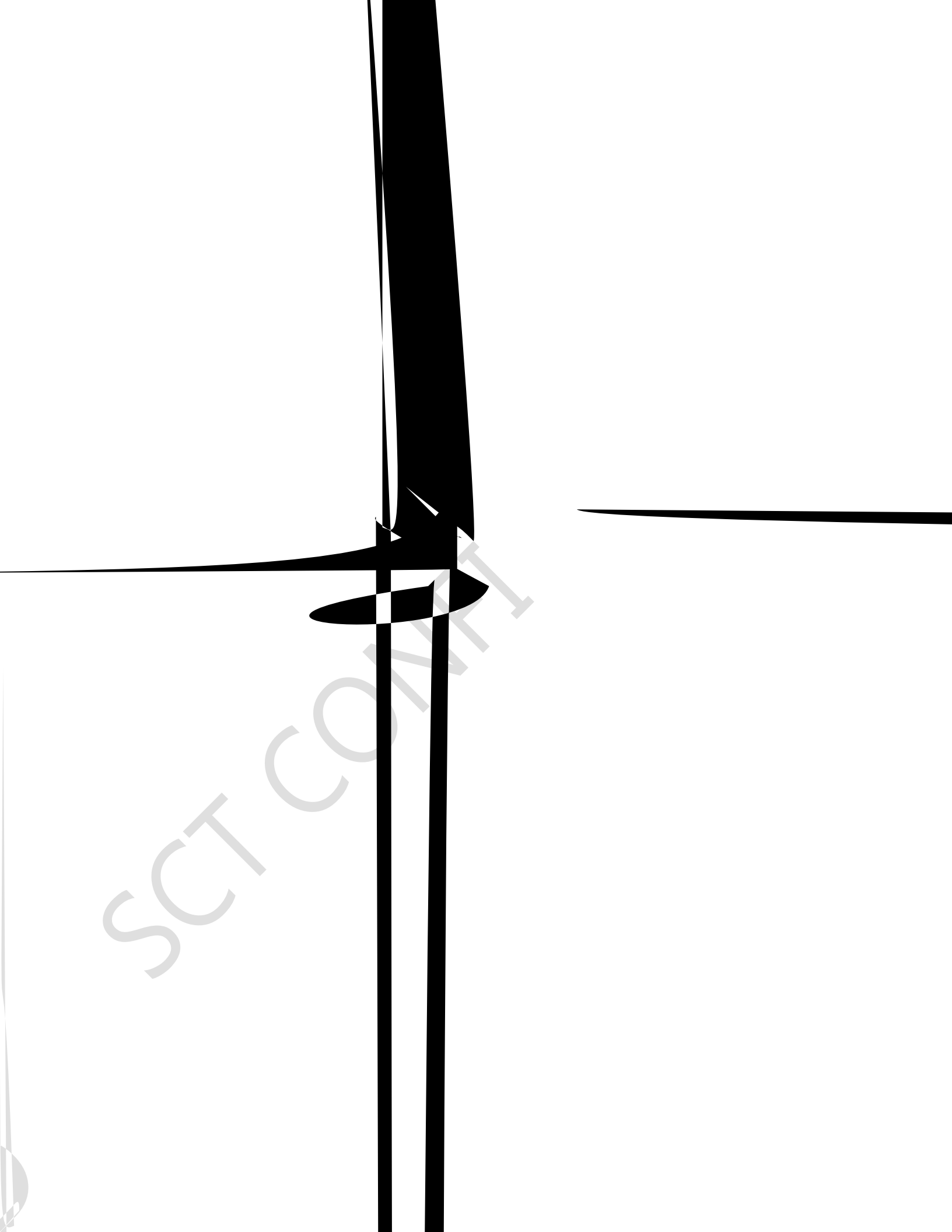
The SCT61242S is available in a 2.5mm×3.5mm QFN-20L package with wettable flanks.

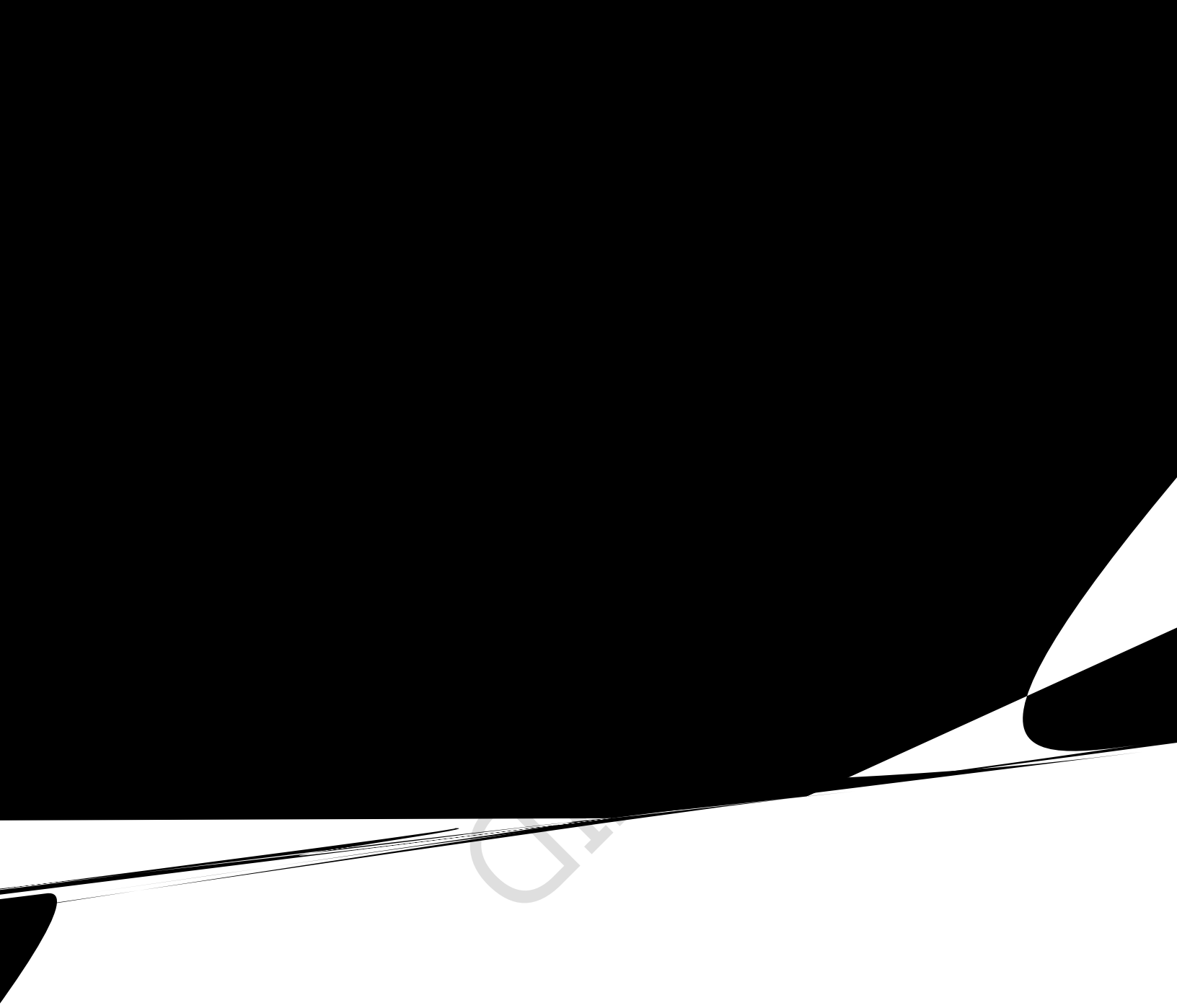
APPLICATIONS

- ADAS
- Compact Camera Module
- Cabin Monitor

TYPICAL APPLICATION







SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
HV BUCK1						
V_{OUT1}	Output voltage configurable range		2.7		5	V
V_{OUT1_ACC}	Output voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C to 150°C	-1.5		1.5	%
R_{DSON_HS1}	High-side MOSFET on-resistance	V_{BST}-V_{SW}=5V		175	350	m
R_{DSON_LS1}	Low-side MOSFET on-resistance			75 Ÿ	side MOSFEETÍìÐ	

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
LDO4						
V_{LDO4}	Output voltage configurable range		1.6		3.5	V
V_{LDO4_ACC}	Output voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C to 150°C	-1.5		1.5	%
V_{LDO4_DROP}	Dropout voltage	V_{OUT1}=3.3V, V_{LDO4} set to 3.3V, I_{LDO4}=300mA		120	300	mV
L_{LINE_REG4}	Line Regulation	V_{OUT1}=3V to 5V, V_{LDO4} set to 2.7V, I_{LDO4}=100mA		0.02		%/V
L_{LOAD_REG4}	Load Regulation	V_{OUT1}=3.3V, V_{LDO4} set to 2.8V, I_{LDO4}=10mA to 300mA		0.1		%
I_{LIM_OCP4}	Over-current limit	V_{OUT1}=3.3V, V_{LDO4} set to 2.8V	320	400	500	mA
I_{LIM_SCP4}	Short-circuit current limit	V_{OUT1}=3.3V, V_{LDO4}=0V	40	70	100	mA
PSRR(1)	Power supply rejection ratio	V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, @ 10kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, @ 100kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, @ 1MHz		40		dB
N_{RMS}(1)	RMS Noise	V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, from 10Hz to 100kHz		30		V_{RMS}
R_{DIS4}	Output discharge resistance	Output disabled		50	100	
Protection						
V_{OV_R}	Output over-voltage rising threshold	OVUVx[1:0]=01	103.5	105	106.5	%
		OVUVx[1:0]=10	104.5	106	107.5	%
		OVUVx[1:0]=11	106.5	108	109.5	%
V_{OV_HYS}	Output over-voltage hysteresis	OVUVx[1:0]=01/10		1		%
		OVUVx[1:0]=11		2		%
V_{UV_F}	Output under-voltage falling threshold	OVUVx[1:0]=01	93.5	95	96.5	%
		OVUVx[1:0]=10	92.5	94	95.5	%
		OVUVx[1:0]=11	90.5	92	93.5	%
V_{UV_HYS}	Output under-voltage hysteresis	OVUVx[1:0]=01/10		1		%
		OVUVx[1:0]=11		2		%
V_{DPOV_R}	Output deep over-voltage protection rising threshold	DEEP_OVP_SEL[1:0]=00		115		%
		DEEP_OVP_SEL[1:0]=01		112		%
		DEEP_OVP_SEL[1:0]=10		110		%
		DEEP_OVP_SEL[1:0]=11		108		%
V_{DPOV_HYS}	Output deep over-voltage protection hysteresis			2		%
V_{DPUV_F}	Output deep under-voltage protection falling threshold	DEEP_UVP_SEL[1:0]=00		75		%
		DEEP_UVP_SEL[1:0]=01		80		%
		DEEP_UVP_SEL[1:0]=10		85		%
		DEEP_UVP_SEL[1:0]=11		90		%

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
		GPIO2_DLYF[1:0]=01	25	40	55	us
		GPIO2_DLYF[1:0]=10	12.5	20	27.5	us
		GPIO2_DLYF[1:0]=11	6.25	10	13.75	us
I2C Interface(1)						
V_{IH}	High level input voltage		1.2			V
V_{IL}	Low level input voltage				0.4	V
V_{OL}	Low level output voltage	I_{SINK}=4mA			0.4	V
f_{SCL}	SCL clock frequency				1	MHz
t_{LOW}	Low period of the SCL clock		500			ns
t_{HIGH}	High period of the SCL clock		260			ns
t_{HD_STA}	Hold time (repeated) START condition		260			ns
t_{SU_STA}	Set-up time for a repeated START condition		260			ns
t_{HD_DAT}	Data hold time		0			ns
t_{SU_DAT}	Data set-up time		50			ns
t_{SU_STO}	Set-up time for STOP condition		260			ns
t_r	Rise time of both SCL and SDA signals				120	ns
t_f	Fall time of both SCL and SDA signals				120	ns
C_B	Capacitive load for each bus line				550	pF

(1) Guaranteed by sample characterization, not tested in production.

TYPICAL CHARACTERISTICS

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, L1 = 2.2uH, L2 = L3 = 1uH, FCCM, T_A = 25°C, unless otherwise noted.

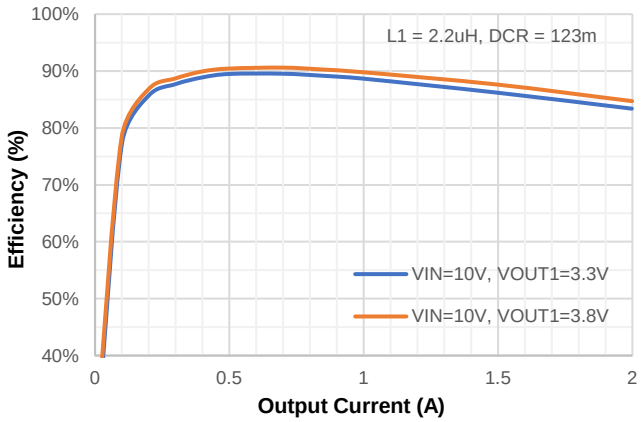


Figure 1. Buck1 Efficiency vs. Load Current

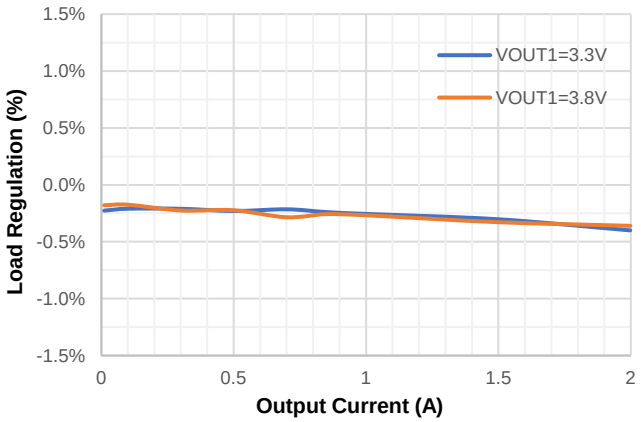


Figure 2. Buck1 Load Regulation

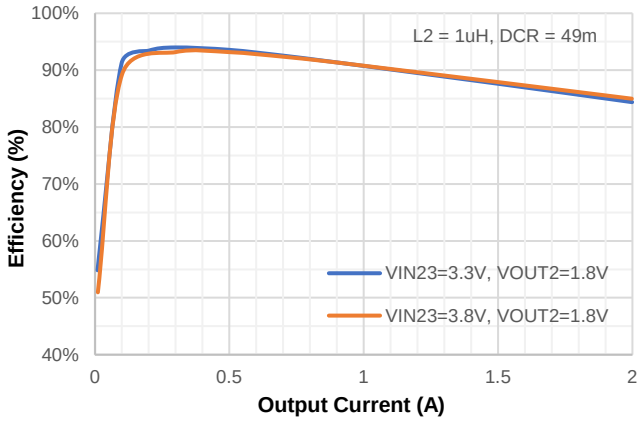


Figure 3. Buck2 Efficiency vs. Load Current

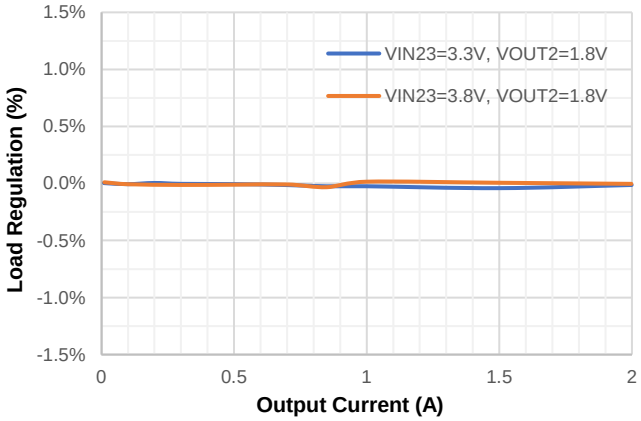


Figure 4. Buck2 Load Regulation

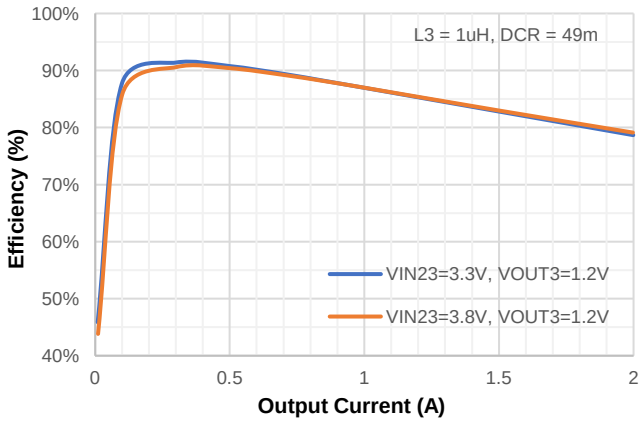


Figure 5. Buck3 Efficiency vs. Load Current

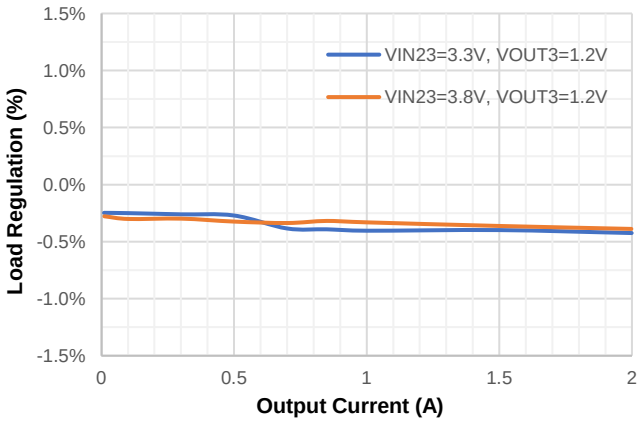


Figure 6. Buck3 Load Regulation

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, L1 = 2.2uH, L2 = L3 = 1uH, FCCM, T_A = 25°C, unless otherwise noted.

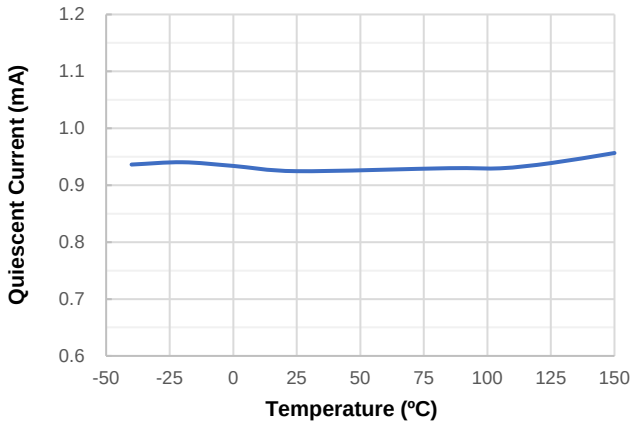


Figure 7. Quiescent Current (rails off) vs. Temperature

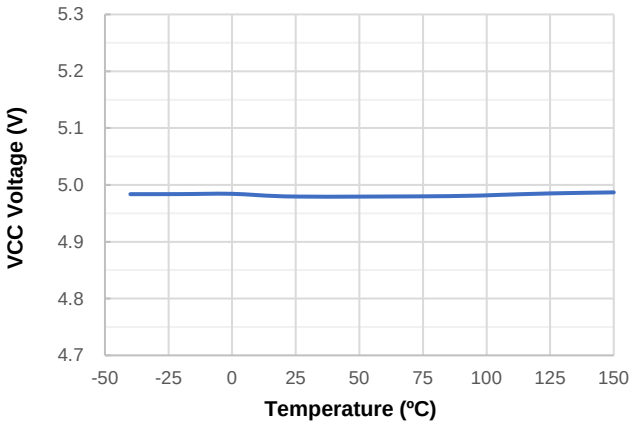


Figure 8. VCC Voltage vs. Temperature

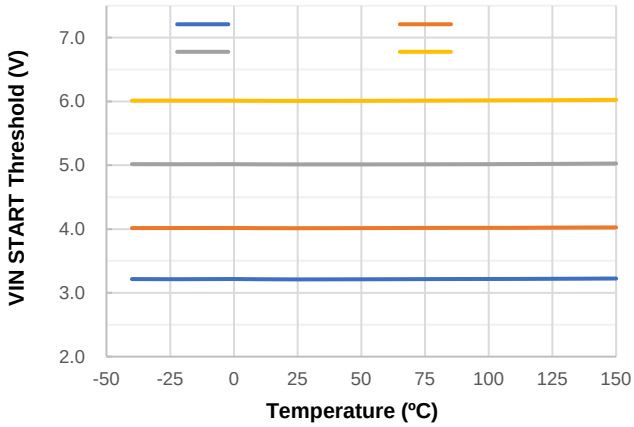


Figure 9. VIN START Threshold vs. Temperature

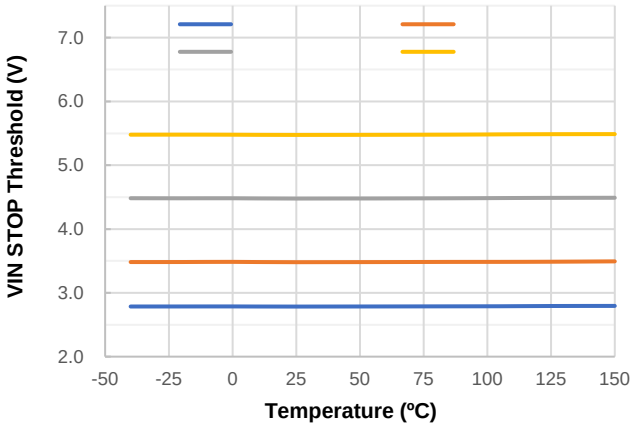


Figure 10. VIN STOP Threshold vs. Temperature

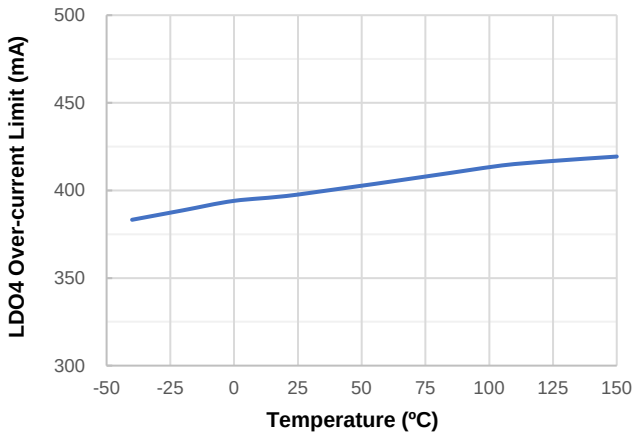


Figure 11. LDO4 Over-current Limit vs. Temperature

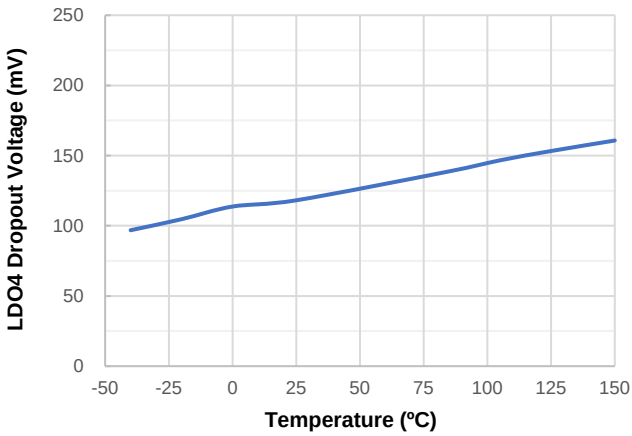
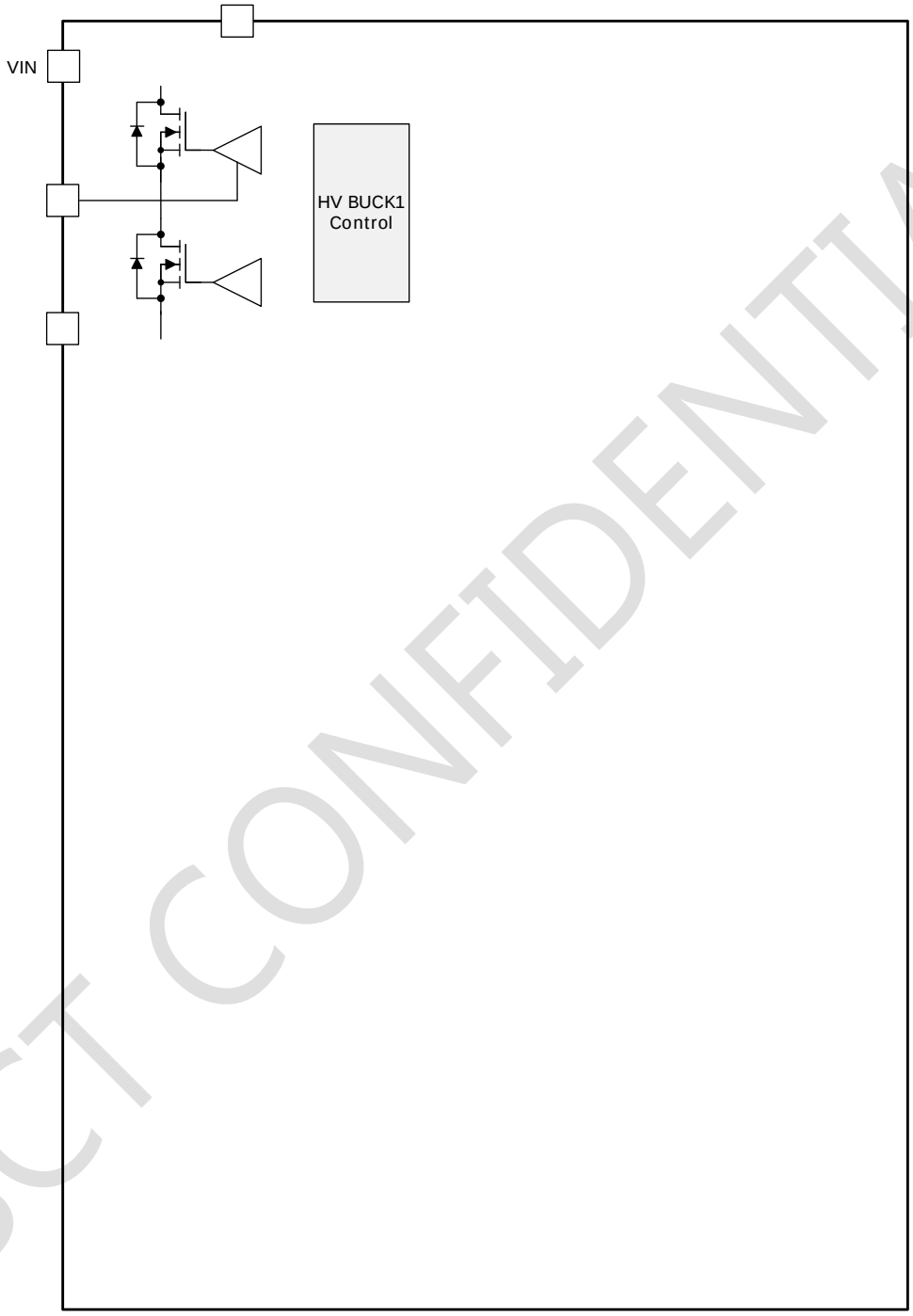


Figure 12. LDO4 Dropout Voltage vs. Temperature

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Overview

The SCT61242S is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high-efficiency synchronous buck converters (HV Buck1, LV Buck2 and LV Buck3) and one high-PSRR, low noise LDO (LDO4) with OV/UV monitoring and flexible power sequence for all outputs.

Buck1 has an input voltage range from 3.5 to 19V for connection to Power over Coax (PoC). Buck2 and Buck3 are identical and powered from the output of Buck1. All three buck converters can operate in either FCCM or PSM mode at light load, with 2.2MHz switching frequency and optional Frequency Spread Spectrum (FSS) function for EMI mitigation. LDO4 is a high PSRR, low noise LDO designed for analog power rail with a continuous output current of up to 300mA. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution.

The SCT61242S is featured with two configurable GPIO pins for flexible system management. GPIO1 can be configured to INTB (interrupt output) or VMON (external voltage monitor input). GPIO2 can be configured to SEQOUT (sequential output for external enable), PG (power good output), GPO (register-based output), INTB, ERRIN (logic input for power cycle), WDI (watchdog input), SLEEPB (sleep mode input) and RSTIN (logic input for reset). For instance, GPIO1 could be configured as VMON while GPIO2 configured as SEQOUT, in which case an external power rail is used, monitored and controlled. The two GPIO pins supports open-drain output and push-pull output of either 1.8V or 3.3V level. Fail-safe feature is also integrated to avoid any unexpected current sinking.

The SCT61242S integrated protection features including input under-voltage protection, input over-voltage protection, output over-voltage/under-voltage protection, over-current protection and thermal shutdown.

The SCT61242S provides Built-in Self Test (BIST) diagnosis over internal analog and digital circuits. All critical comparator and data will be checked at power-up stage. Watchdog is also supported to further improve system safety. The watchdog could be fed by periodic trigger pulse or specific I2C write operation with programmable timing window. Safety features ensure compliance with ISO26262 standard and functional safety up to ASIL-C level.

Operating State Machine

The operation state machine of SCT61242S is shown in Figure 14. The power rail action and system function in each state are listed in Table 1.

Table 1. PMIC Operation in Each State

<table>
<tr><th rowspan="2">State</th><th colspan="4">Power Rail</th><th colspan="5">Function</th></tr>
<tr><th>Buck1</th><th>Buck2</th><th>Buck3</th><th>LDO4</th><th>RESETB</th><th>I2C</th><th>Watchdog</th><th>TSD</th><th>Register</th></tr>
<tr><td>IDLE</td><td rowspan="6">OFF</td><td rowspan="6">OFF</td><td rowspan="6">OFF</td><td rowspan="6">OFF</td><td>Hi-Z</td><td rowspan="3">OFF</td><td rowspan="6">OFF</td><td rowspan="3">OFF</td><td>Reset</td></tr>
<tr><td>LOADOTP(PRE)</td><td rowspan="5">Low</td><td rowspan="5">\</td></tr>
<tr><td>LBIST</td></tr>
<tr><td>LOADOTP</td><td rowspan="3">ON</td></tr>
<tr><td>STANDBY</td><td>ON</td></tr>
<tr><td>ABIST</td><td>OFF</td></tr>
<tr><td>POWERUP</td><td rowspan="5">ON</td><td rowspan="3">ON</td><td rowspan="3">ON</td><td rowspan="3">ON</td><td rowspan="3">ON</td></tr>
<tr><td>NORMAL</td><td>High</td><td>ON</td></tr>
<tr><td>RESET</td><td>Low</td><td>OFF</td></tr>
<tr><td>SLEEP</td><td>ON/OFF</td><td>ON/OFF</td><td>ON/OFF</td><td rowspan="2">High</td><td>OFF</td><td rowspan="2">ON</td><td rowspan="4">ON</td></tr>
<tr><td>RECOVER</td><td rowspan="2">ON</td><td rowspan="2">ON</td><td rowspan="2">ON</td><td rowspan="3">ON</td></tr>
<tr><td>RCVRST</td><td rowspan="3">Low</td><td rowspan="3">OFF</td></tr>
<tr><td>DEEPSAFE</td><td rowspan="2">OFF</td><td rowspan="2">OFF</td><td rowspan="2">OFF</td><td rowspan="2">OFF</td></tr>
<tr><td>TURNOFF</td></tr>
</table>

LBIST State

The diagnostics of the monitoring and protection circuits in the digital core is performed by LBIST. LBIST is implemented in this state and any error found will be recorded in register bit **LBIST_ERR[0]**. When LBIST is completed, the device transits to LOADOTP state. There is a tradeoff between LBIST diagnostic coverage and running time and the default LBIST duration is around 2ms.

LOADOTP State

The device will load data from OTP to corresponding registers and implement OTP CRC again after LBIST, then STANDBY state is entered.

STANDBY State

STANDBY state is where the device could be held on to check and wait for all conditions met to power up. To exit STANDBY state, VIN shall be higher than V_{IN_START} threshold, output rails shall be discharged, LBIST and OTP CRC shall pass and no other critical fault like thermal shutdown is triggered. The device will transit to ABIST state almost immediately if all conditions are met when entering STANDBY state.

ABIST State

To ensure safety mechanism works well, the device will check through all critical analog comparators before power rails built up. ABIST(Analog Built-in Self Test) will be implemented every time the device enters ABIST state. If ABIST check fails, the device will transit to DEEPSAFE state, and if ABIST passes, the device will transit to POWERUP state. Any error found during ABIST will be recorded in register bit **ABIST_ERR[0]**.

POWERUP State

In POWERUP state, all power rails will be built up following a dedicated OTP-programmed sequence. Since HV Buck1 is the power supply for the other channels, Buck1 is always set to start up first. The other channels then will start up with their own turn-on delay time configuration respectively, which is configured in register **CONFIG_SEQ45** and **CONFIG_SEQ23**. See Figure 20 for a detailed power up sequence. If all channels finish soft-start within power good range, the RESETB rising delay timer starts. Once the timer is expired, the device will enter NORMAL state and RESETB pin will be pulled high. If any deep safe event occurs, the device will transit to DEEPSAFE state directly.

NORMAL State

NORMAL state is the normal operation state of the device with all enabled channels on. RESETB pin is pulled high upon entering this state. If watchdog is enabled in register **CONFIG_WD3**, the watchdog window cycle will be initiated and watchdog shall be fed by periodic trigger pulse through GPIO2 as WDI or specific I2C write operation at correct timing. SLEEP state could be entered if **EN_LP[0]**=1 and SLEEPB is pulled low when GPIO2 configured as SLEEPB, where low power mode is activated and a very low standby current is achieved. When operating in NORMAL state, the device will transit to RESET state once any reset event occurs.

RESET State

All power rails keep on with just RESETB pin pulled low in RESET state. The device transits from NORMAL state to RESET state when any of the reset events shown in Table 2 occurs. When the device enters RESET state, RESETB pin will be pulled low for a hold time configured in **RESETB_HT[1:0]**. The device will go back to NORMAL state once the hold time expired and the reset event discontinued. The watchdog error counter is reset and watchdog window cycle is initiated when transiting from RESET to NORMAL state. If some reset events are not needed or undesired, the device provides corresponding mask options in register **CTRL_FLTMAP1** and **CTRL_FLTMAP2**.

Table 2. Reset Event

Category	Reset Event	Map/Mask Bit	Status Bit
Analog	Buck1 output is out of OV/UV range	RSTMAP_VO1[0]	OV1[0], UV1[0]
	Buck2 output is out of OV/UV range	RSTMAP_VO2[0]	OV2[0], UV2[0]
	Buck3 output is out of OV/UV range	RSTMAP_VO3[0]	OV3[0], UV3[0]
	LDO4 output is out of OV/UV range	RSTMAP_VO4[0]	OV4[0], UV4[0]
	VMON input is out of OV/UV range (when GPIO1 configured as VMON)	RSTMAP_VMON[0]	OV5[0], UV5[0]
	VMON deep OVP/UVP (when VMON_DEEPSAFE_CTRL[0]=1)	RSTMAP_VMONDP[0]	DEEPOVP5[0], DEEPUVP5[0]
	VIN OVP (when VINOVP_DEEPSAFE_CTRL[0]=1)	RSTMAP_VINOVP[0]	VIN_OVP[0]
Digital	Watchdog failure	RSTMAP_WD[0]	WD_ERR[0]
	I2C PEC error	RSTMAP_I2C[0]	I2C_PEC_ERR[0]
	RSTIN input high (when GPIO2 configured as RSTIN)	RSTMAP_RSTIN[0]	RSTIN[0]
	Internal clock error	\	CLK_MON_ERR[0]
	GPIO1/2 monitor error	\	GPIO1_OUT_ERR[0], GPIO2_OUT_ERR[0]

SLEEP State

The device provides a low-power sleep mode where each channel could be configured to turn off or operate in PSM to reduce power consumption. The device transits from NORMAL state to SLEEP state when **EN_LP[0]** is set to 1 and SLEEPB is pulled low (GPIO2 configured as SLEEPB). RESETB pin remains high and I2C operation is disabled in SLEEP state. Once SLEEPB is pulled high, the device will be awakened, going through RECOVER state and back to NORMAL state with **EN_LP[0]** self-cleared to 0.

RECOVER State

RECOVER state is an intermediate state when the device is awakened from SLEEP state. The channels disabled in SLEEP state will start up with the turn-on delay time same as in POWERUP state, and other channels will resume to FCCM operation. After all outputs are built up successfully, the device will enter NORMAL state. If any reset event triggered in RECOVER state, the device goes to RCVRST state.

RCVRST State

RCVRST state is an extra reset state to assert RESETB pin with output rails keep starting up in programmed sequence. This state aims to allow possible reset events to be triggered for those continuously enabled rails, like an output OV/UV. The device will go back to RECOVER state automatically once the hold time expired and the reset event discontinued.

TURNOFF State

If the device is manually turned off (e.g., writing **EN_ALL[0]**=0 online), or VIN drops to lower than V_{IN_STOP} threshold after start-up, TURNOFF state will be entered. All channels will be shut down with their turn-off delay time configuration in register **CONFIG_SEQ45** and **CONFIG_SEQ23**. See Figure 21 for a detailed power down sequence. After power down sequence is finished, the device will go back to STANDBY state waiting for reboot. If any deep safe event triggered in TURNOFF state, the device transits to DEEPSAFE state.

DEEPSAFE State

In DEEPSAFE state, all channels are shut off and RESETB pin is pulled low. Regardless of current state, the device can always jump to DEEPSAFE state when any of the deep safe events shown in Table 3 occurs after start-up. All power rails are shut down immediately and simultaneously while I2C interface keeps alive in DEEPSAFE state,

allowing user to communicate with the device and read the status registers to locate the specific fault. The device will go back to STANDBY state once the hiccup timer expired and the deep safe event discontinued.

Table 3. Deep Safe Event

Category	Deep Safe Event	Status Bit
Analog	Buck1 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP1[0], DEEPUVP1[0], UV1[0], OC1[0]
	Buck2 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP2[0], DEEPUVP2[0], UV2[0], OC2[0]
	Buck3 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP3[0], DEEPUVP3[0], UV3[0], OC3[0]
	LDO4 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP4[0], DEEPUVP4[0], UV4[0], OC4[0]
	VMON deep OVP/UVP (when VMON_DEEPSAFE_CTRL[0]=0)	DEEPOVP5[0], DEEPUVP5[0],
	VIN OVP (when VINOVP_DEEPSAFE_CTRL[0]=0)	VIN_OVP[0]
	VCC OVP	VCC_OVP[0]
	POWERUP/RECOVER state timeout	POWERUP_TIMEOUT[0]
	Ground loss	GND_LOSS[0]
	Thermal shutdown	THSD[0]
	ABIST error	ABIST_ERR[0]
Digital	Online CRC error	ONLINE_CRC_ERR[0]
	RESETB monitor error	RESETB_MON_ERR[0]
	Power sequence error	SEQ_ERR[0]
	ERRIN input high (when GPIO2 configured as ERRIN)	ERRIN[0]

High Efficiency Regulators

All three buck converters employ 2.2MHz fixed frequency peak current mode control. Optional Forced Continuous Conduction Mode (FCCM) ensures good output performance at light-load, or Pulse Skip Mode (PSM) to provide excellent light-load efficiency. HV Buck1 is always the first one to power up, LV Buck2 and LV Buck3 then will start up with corresponding turn-on delay time configuration. The soft-start time is fixed at 0.8ms for all three buck converters.

Buck1 is a high-voltage synchronous buck converter directly powered from VIN pin. Buck1 output can be regulated at 2.7V to 5V with down to 100mV steps, providing a continuous output current of up to 2A. An external 100nF ceramic capacitor between BST and SW1 pins is required to power high-side power MOSFET gate driver, which is charged from VCC when low-side power MOSFET is on. Buck1 output is the power supply for other channels.

Buck2 and Buck3 are two identical low-voltage synchronous buck converter powered by Buck1. Both Buck2 and Buck3 output can be regulated at 0.6V to 2.15V with 50mV steps, providing up to 2A continuous output current. To further improve the EMI performance, Buck2 and Buck3 will operate in 180° phase shift.

LDO4 is a high PSRR, low noise LDO designed for analog power rail, also powered from Buck1. LDO4 output can be regulated at 1.6V to 3.5V with 50mV steps, providing a continuous output current of up to 300mA.

All output voltages are pre-programmed without any external feedback divider, and continuously monitored during operation. There is a two-stage OV/UV protection strategy. The over-voltage and under-voltage threshold of each channel can be configured independently in **OVUVx[1:0]**. Any output OV/UV condition will trigger a reset event to pull RESETB pin low. For worse OV/UV cases, deep over-voltage protection or deep under-voltage protection will kick in to shut down all channels, as a deep safe event.

Deep Over-voltage Protection

If any output voltage exceeds the deep over-voltage protection threshold configured in **DEEP_OVP_SEL[1:0]** during operation, a deep safe event is triggered and all outputs will be shut down for the hiccup time. In this hiccup time, all output rails will be discharged by internal circuit. When the hiccup timer expired and the deep over-voltage

RESETB Indicator

The RESETB pin will assert when any reset event or deep safe event occurs. The RESETB output could be configured to be either open-drain or push-pull by **RESETB_OUT[0]**, and the high level of push-pull mode could be set to either 1.8V or 3.3V by **VIO[0]**, with an internal resistance of around 1k . To avoid some reset events triggering RESETB, the device provides mask options in register **CTRL_FLTMAP1** and **CTRL_FLTMAP2**. A deep safe event will always pull RESETB low.

General Purpose I/O

The SCT61242S is featured with two configurable GPIO pins for flexible system management. Each GPIO could be configured to a dedicated function pin as either input or output for different applications. GPIO1 can be configured to INTB or VMON. GPIO2 can be configured to SEQOUT, PG, GPO, INTB, ERRIN, WDI, SLEEPB and RSTIN. See Table 4 for a detailed description.

Table 4. GPIO Configuration

Pin	I/O	Function	Description
GPIO1	Input	VMON	External voltage monitor input. VMON can be used to monitor the external regulator output voltage with configurable activation timing.

Watchdog

The SCT61242S provides two kinds of watchdog operation mode, simple watchdog and Question and Answer (QA) watchdog.

In simple watchdog mode, watchdog is fed by trigger pulse to WDI(GPIO2) pin, or writing any byte to register **WD_KEY**. Once the device enters NORMAL state, the watchdog will be activated starting by close window and followed by open window, with extension cycles configured by **WD_1UD[0]**. The duration of close window and open window in each cycle could be configured by **WD_TCLOSE[3:0]** and **WD_TOPEN[3:0]**, and watchdog shall be fed only within open window. A correct watchdog feed action will restart the whole window cycle immediately. If watchdog fed during close window, status bit **WD_UV[0]** will be set, the watchdog error counter will be incremented and the window cycle will also be refreshed. Any feed action during the first close window after NORMAL state entered will be blanked. If watchdog not fed before open window expired, status bit **WD_EXP[0]** will be set, the watchdog error counter will be incremented and the window cycle will be refreshed. When watchdog error counter reaches the times configured in **WD_FAIL_CNT[1:0]**, a reset event will be triggered and status bit **WD_ERR[0]** will be set. The device transits to RESET state and goes back to NORMAL state after a hold time. The watchdog error counter is reset and watchdog window cycle is initiated when transiting from RESET back to NORMAL state.

I2C Interface

The SCT61242S integrates a two-wire serial interface for bidirectional communications between the device and the master through the bus. The I2C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The SCT61242S is assigned a unique chip address 0x38 and operates as a slaver. The master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and the SDA lines need a pull-up resistor connected to bus voltage since high state is the default state when bus is idle. The SCT61242S supports Standard mode (up to 100kHz), Fast-mode (up to 400kHz) and Fast-mode Plus (up to 1MHz). The internal filtering ignores spikes and noises on the bus line to preserve data integrity. The maximum capacitive load for each bus line is given in Electrical Characteristic thus the number of Interfaces is limited.

Data Validity

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low.

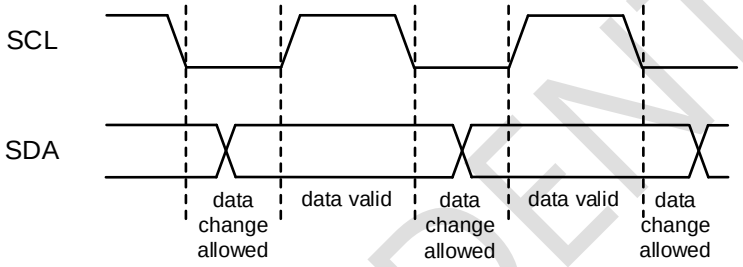


Figure 17. Data Validity Diagram

START and STOP Conditions

The data transfer always generates START and STOP conditions to announce the process. A high to low transition on the SDA line while SCL is high defines a START condition. A low to high transition on the SDA line while SCL is high defines a STOP condition. Both the START and STOP conditions are generated by the master on the bus.

The bus is considered to be busy after START condition and released after STOP condition. A repeated START condition during transmission is also valid and will be regard as a new START condition.

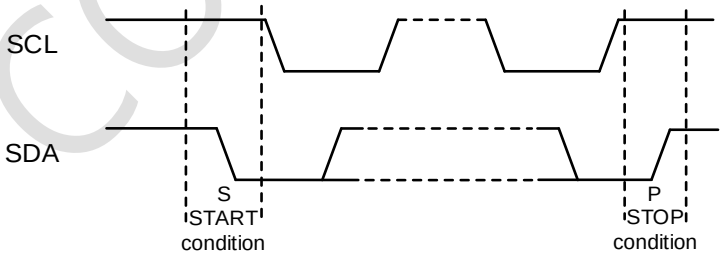


Figure 18. START and STOP Conditions Diagram

Data Transmission

The transferred byte consists of eight bits with the Most Significant Bit (MSB) first. After each byte is transferred, the master will release the SDA line and generate the ninth acknowledge clock pulse on SCL line. The SCT61242S will pull the SDA line low during this acknowledge clock, to announce a successful reception and next byte may be sent. If the master is receiver and the last byte is received, it still generates the ninth acknowledge clock pulse but SDA line will not be pulled low. It's called not acknowledge signal and indicates the end of transmission.

After the START condition, the master must send a slave address as the first addressing byte. The slave address is seven bits long followed by an eighth R/W bit. The R/W bit defines the data direction. Set the R/W bit to 0 to indicate write command, and a 1 indicates read command.

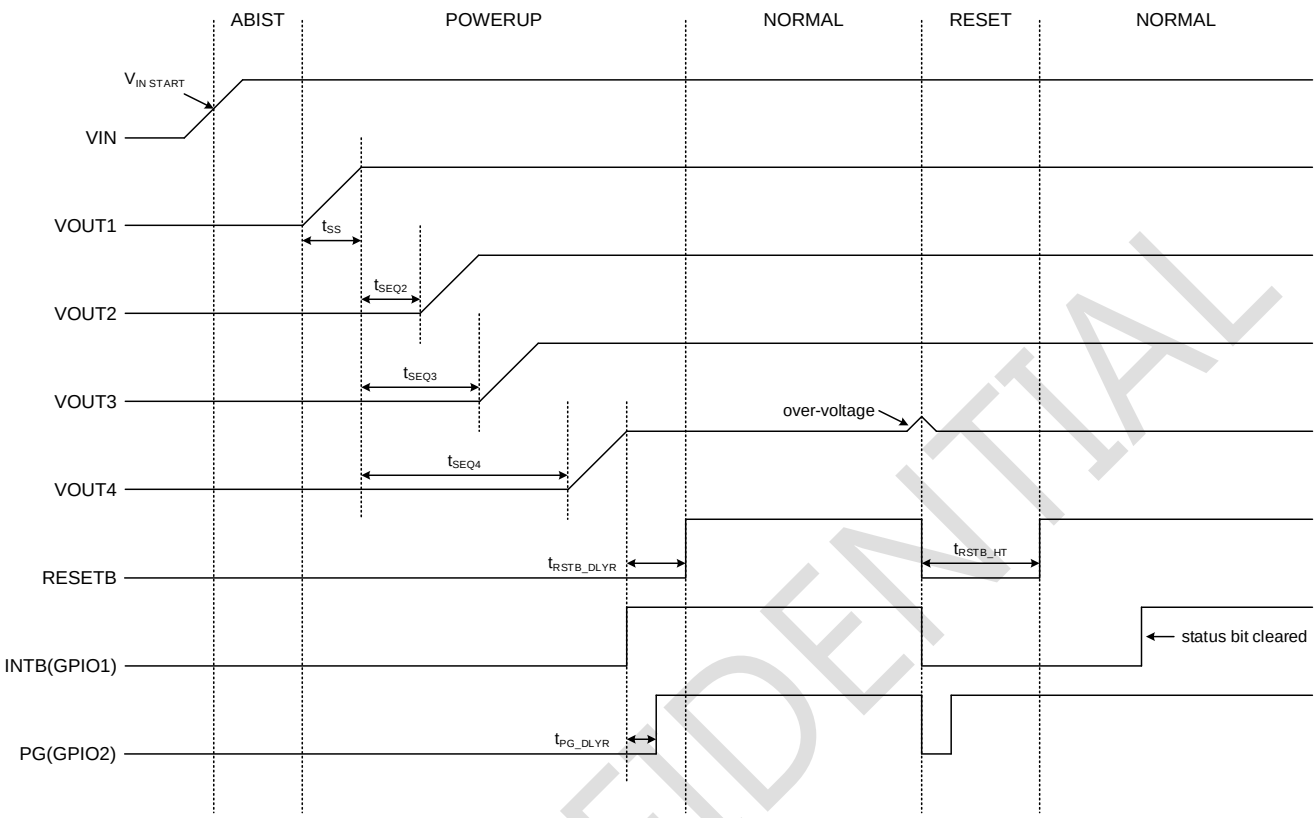


Figure 20. Power Up Sequence

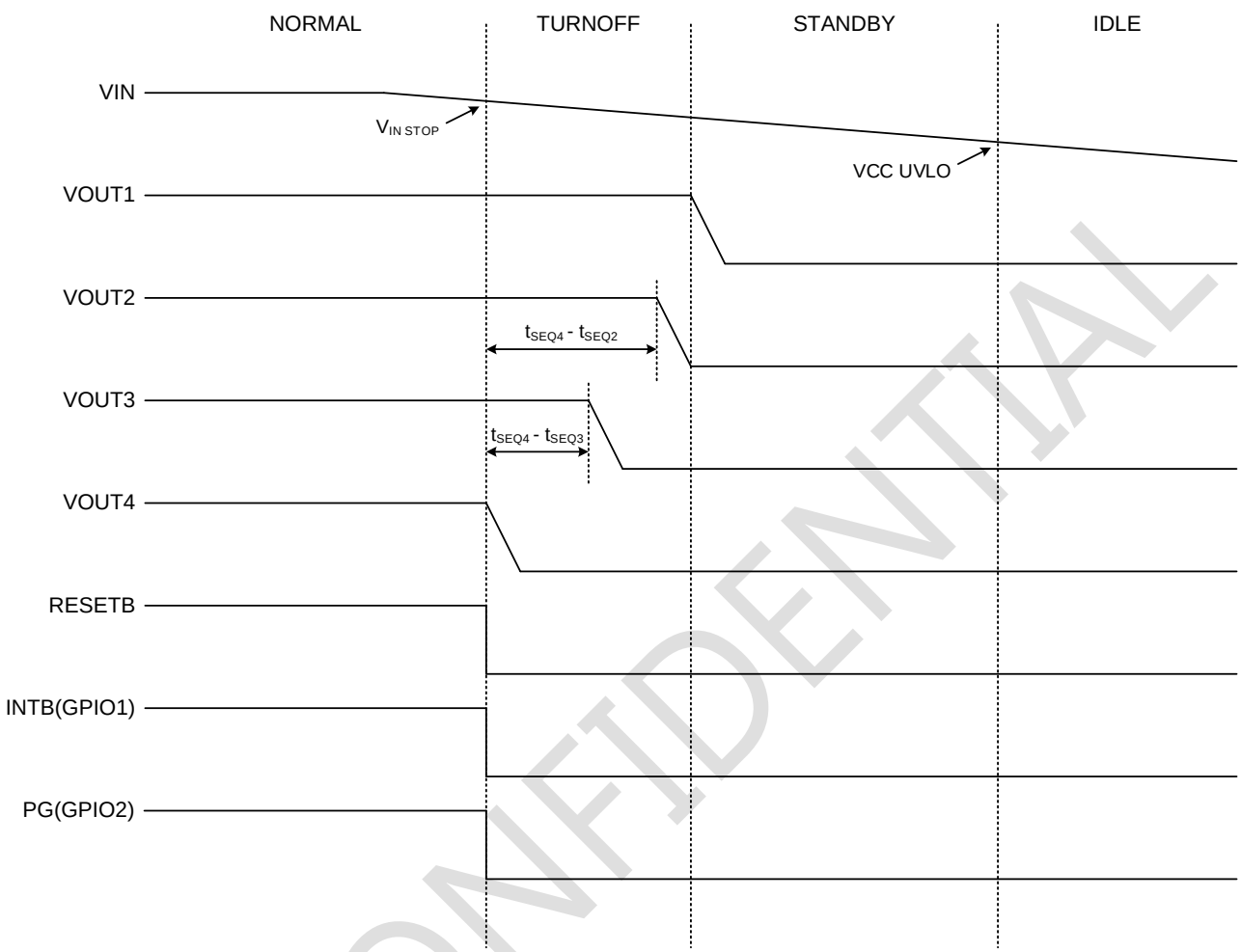


Figure 21. Power Down Sequence

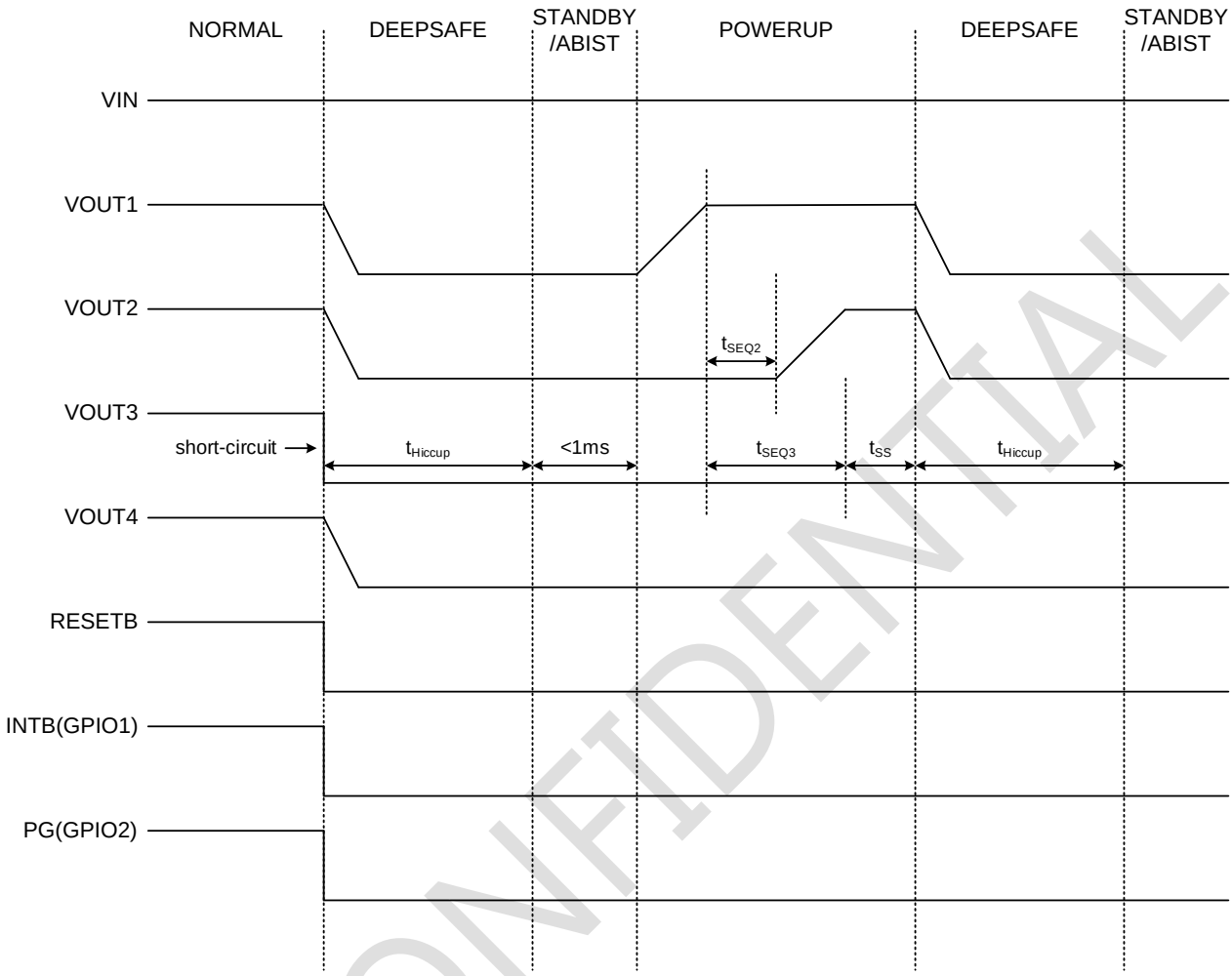


Figure 22. Deep Safe Event

APPLICATION INFORMATION

Typical Application

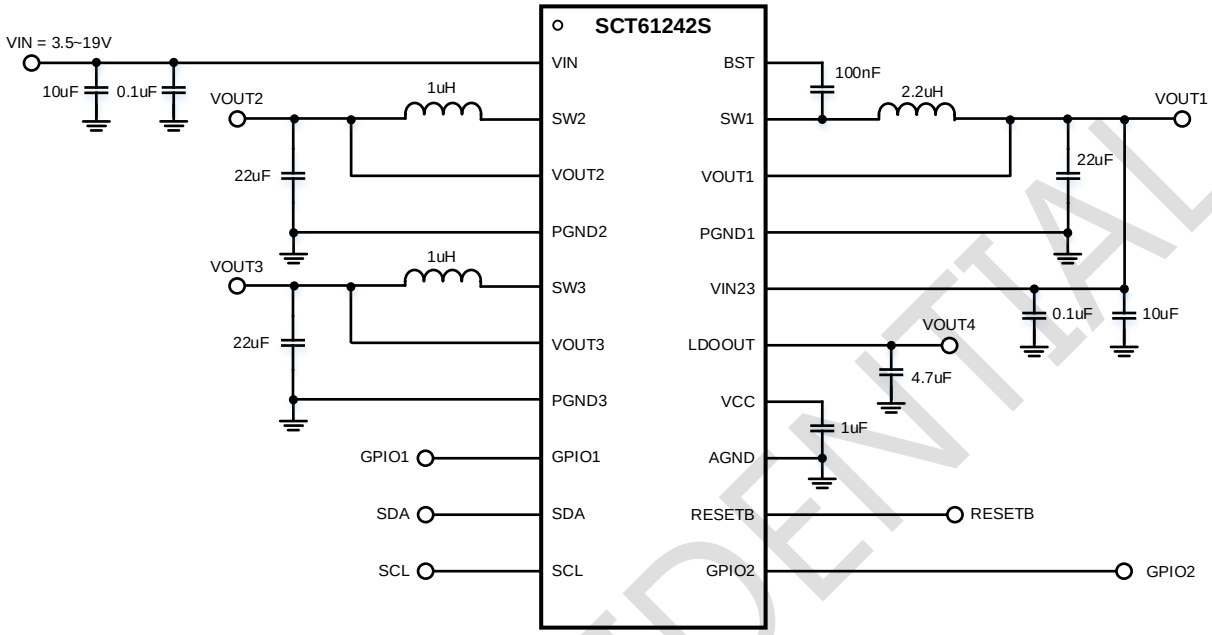


Figure 23. Application Schematic, 3.5V to 19V Input

Design Parameters	Example Value
Input Voltage	Nominal 10V
Output Voltage	Buck1: 3.3V Buck2: 1.8V Buck3: 1.2V LDO4: 2.8V
Maximum Output Current	Buck1: 2A Buck2: 2A Buck3: 2A LDO4: 300mA
Switching Frequency	2.2MHz
Output Voltage Ripple (Peak-to-Peak)	Buck1: <10mV Buck2: <5mV Buck3: <5mV

The SCT61242S is featured with minimized external components and all feedback divider, pull-up or configuration resistor could be saved. For typical application, the recommended inductance and capacitance for each power rail are listed in Table 6. Higher inductance and capacitance for lower output ripple are also acceptable.

Table 6. Recommended BOM for Typical Application

Output Rail	Switching Frequency	Inductor	Output Capacitor
Buck1	2.2MHz	2.2uH	10uF or 22uF
Buck2	2.2MHz	1uH	10uF or 22uF
Buck3	2.2MHz	1uH	10uF or 22uF
LDO4	-	-	4.7uF

Application Waveforms

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, L1 = 2.2uH, L2 = L3 = 1uH, FCCM, T_A = 25°C, unless otherwise noted.

Figure 24. Power Up Sequence

Figure 25. Power Down Sequence

Figure 26. Buck1 Steady State, Load=1A

Figure 27. Buck2 Steady State, Load=1A

Figure 28. Buck3 Steady State, Load=1A

Figure 29.

Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over-heat area.
2. Place a low ESR ceramic capacitor as close to VIN and VIN23 pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. Connect AGND to PGND plane at a single point.

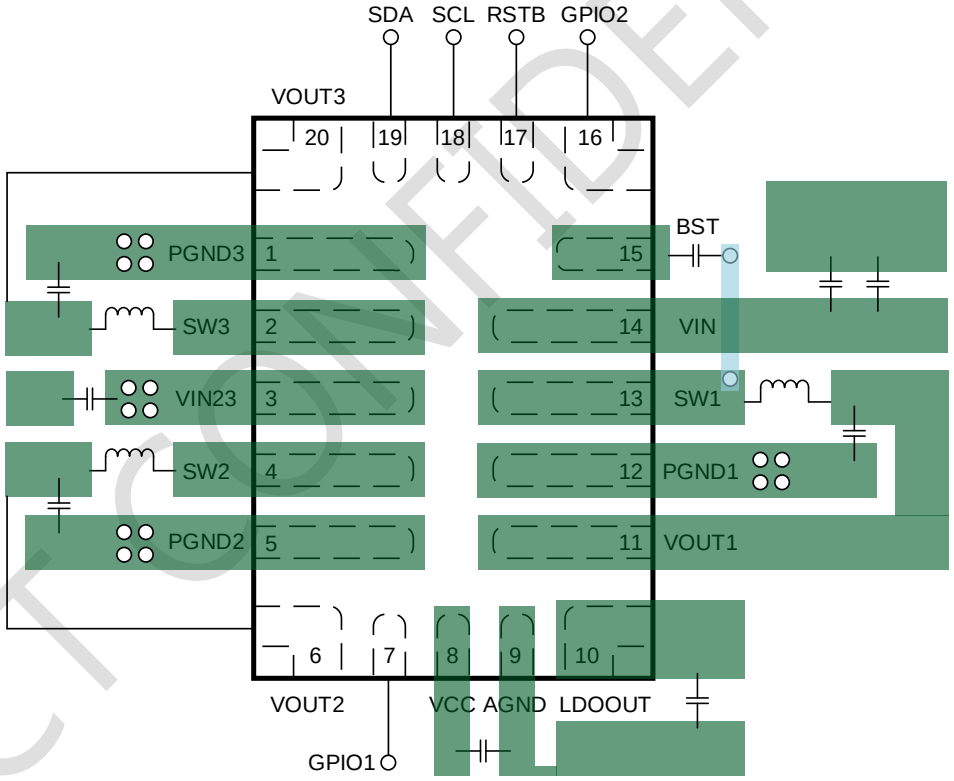


Figure 30. PCB Layout Example

REGISTER MAP

ADDRESS	REGISTER	DEFAULT VALUE	OTP ACCESS	I2C WRITE LOCK
0x00	CHIPID	-	Y	-
0x01	CTRL_EN	-	Y	Y
0x02	CTRL_ENLP	-	Y	Y
0x03	CONFIG_SYSTEM	-	Y	-
0x04	CONFIG_BUCK1	-	Y	-
0x05	CONFIG_BUCK2	-	Y	-
0x06	CONFIG_BUCK3	-	Y	-
0x07	CONFIG_LDO4	-	Y	-
0x08	CONFIG_VMON	-	Y	-
0x09	CONFIG_MISC	-	Y	-
0x0A	CONFIG_T1	-	Y	-
0x0B	CONFIG_T2	-	Y	-
0x0C	CONFIG_SEQ45	-	Y	-
0x0D	CONFIG_SEQ23	-	Y	-
0x0E	CONFIG_WD1	-	Y	N
0x0F	CONFIG_WD2	-	Y	N
0x10	CONFIG_WD3	-	Y	N
0x11	WD_KEY	-	N	N
0x12	WD_LOCK	-	N	N
0x13	CONFIG_GPIO0	-	Y	-
0x14	CONFIG_GPIO1	-	Y	-
0x15	CTRL_GPO	-	N	Y
0x16	CONFIG_FLTMAP1	-	Y	Y
0x17	CONFIG_FLTMAP2	-	Y	Y
0x18	STATUS1	-	N	N
0x19	STATUS2	-	N	N
0x1A	STATUS3	-	N	N
0x1B	STATUS4	-	N	N
0x1C	STATUS5	-	N	N
0x1D	STATUS6	-	N	N
0x1E	STATE	-	N	N
0xE0	I2C_LOCK	-	N	N
0xE1	CTRL_RESTART	-	N	N
0xE2	CTRL_ONLINE_ABIST	-	N	N

CONFIG_BUCK2 [7:0]			
ADDRESS: 0x05			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	PSM2	R	Buck2 FCCM/PSM mode selection in NORMAL state. 0: FCCM 1: PSM
[6:5]	OVUV2	R	Buck2 output OV/UV threshold selection. 00: Reserved 01: ±5% 10: ±6% 11: ±8%
[4:0]	VOUT2	R	Buck2 output voltage setting. 00000: 0.6V 00001: 0.65V 00010: 0.7V … 01100: 1.2V … 11000: 1.8V … 11110: 2.1V 11111: 2.15V (V_{OUT2} = 0.6V + VOUT2[4:0] × 0.05V)

CONFIG_BUCK3 [7:0]			
ADDRESS: 0x06			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	PSM3	R	Buck3 FCCM/PSM mode selection in NORMAL state. 0: FCCM 1: PSM
[6:5]	OVUV3	R	Buck3 output OV/UV threshold selection. 00: Reserved 01: ±5% 10: ±6% 11: ±8%
[4:0]	VOUT3	R	Buck3 output voltage setting. 00000: 0.6V 00001: 0.65V 00010: 0.7V … 01100: 1.2V … 11000: 1.8V … 11110: 2.1V 11111: 2.15V (V_{OUT3} = 0.6V + VOUT3[4:0] × 0.05V)

CONFIG_LDO4 [7:0]			
ADDRESS: 0x07			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	RESERVED	R	/
[6:5]	OVUV4	R	LDO4 output OV/UV threshold selection. 00: Reserved 01: ±5% 10: ±6% 11: ±8%
[4:0]	VOUT4	R	LDO4 output voltage setting. 00000: 1.6V 00001: 1.65V 00010: 1.7V … 01001: 2.05V 01010: 2.1V (50mV step from 1.6V to 2.1V, V_{OUT4} = 1.6V + VOUT4[4:0] × 0.05V) 01011: 2.5V 01100: 2.55V … 10001: 2.8V … 11011: 3.3V … 11110: 3.45V 11111: 3.5V (50mV step from 2.5V to 3.5V, V_{OUT4} = 2.5V + VOUT4[4:0] × 0.05V)

CONFIG_VMON [7:0]
ADDRESS: 0x08

CONFIG_MISC [7:0]			
ADDRESS: 0x09			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	DEEP_OVP_SEL	R	Deep OVP threshold selection for all channels. 00: 115% 01: 112% 10: 110% 11: 108%
[5:4]	DEEP_UVP_SEL	R	Deep UVP threshold selection fj 0 T2.6 (el)-0.70%

CONFIG_T1 [7:0]			
ADDRESS: 0x0A			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	RESETB_HT	R	RESETB assertion low-level hold time. The RESETB pin is pulled low at least for this duration when any reset event triggered. After the hold time expired, NORMAL state will be entered if the reset event discontinued. 00: 10ms 01: 20ms 10: 30ms 11: 40ms
[5:4]	RESETB_DLYR	R	RESETB rising delay time after all channels are built up in POWERUP state. When RESETB_DLYR_SCALE[0]=0: 00: 0.5ms 01: 1ms 10: 2ms 11: 4ms When RESETB_DLYR_SCALE[0]=1: 00: 2.5ms 01: 5ms 10: 10ms 11: 20ms
[3:2]	PG_DLYR	R	PG rising delay time when GPIO2 is set to PG. 00: 50us 01: 100us 10: 150us 11: 200us
[1:0]	PG_DLYF	R	PG falling delay time when GPIO2 is set to PG. 00: 50us 01: 100us 10: 150us 11: 200us

CONFIG_T2 [7:0]			
ADDRESS: 0x0B			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	ON_DELAY_SCALE	R	Power up sequence on delay time scale selection. 00: t_{ON_SCALE} = 0.5ms (0~7.5ms range) 01: t_{ON_SCALE} = 1ms (0~15ms range) 10: t_{ON_SCALE} = 2ms (0~30ms range) 11: t_{ON_SCALE} = 4ms (0~60ms range)
[5:4]	OFF_DELAY_SCALE	R	Power down sequence off delay time scale selection. 00: t_{OFF_SCALE} = 0.5ms (0~7.5ms range) 01: t_{OFF_SCALE} = 1ms (0~15ms range) 10: t_{OFF_SCALE} = 2ms (0~30ms range) 11: t_{OFF_SCALE} = 4ms (0~60ms range)
[3:0]	OVUV_FILTER_TIME	R	OV rising/UV falling filter time for all output comparators. t_{FILT} = (OVUV_FILTER_TIME[3:0] + 1) × 10us

CONFIG_SEQ45 [7:0]			
ADDRESS: 0x0C			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:4]	SEQ5	R	SEQOUT rising delay time configuration after Buck1 output built in power up sequence. VMON blanking time is initiated after this delay time. It also configures SEQOUT falling delay time. t_{ON_SEQ5} = SEQ5[3:0] × t_{ON_SCALE} t_{OFF_SEQ5} = SEQ5[3:0] × t_{OFF_SCALE}
[3:0]	SEQ4	R	LDO4 turn-on delay time configuration after Buck1 output built in power up sequence. It also configures LDO4 turn-off delay time. See Figure 20 and Figure 21 for details. t_{ON_SEQ4} = SEQ4[3:0] × t_{ON_SCALE} t_{OFF_SEQ4} = SEQ4[3:0] × t_{OFF_SCALE}

CONFIG_SEQ23 [7:0]			
ADDRESS: 0x0D			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:4]	SEQ3	R	Buck3 turn-on delay time configuration after Buck1 output built in power up sequence. It also configures Buck3 turn-off delay time. See Figure 20 and Figure 21 for details. .44 T Q q 245.76 186.12 [illegible] t_{OFF_SEQ3} = SEQ3[3:0] × t_{OFF}

CONFIG_WD1 [7:0]			
ADDRESS: 0x0E			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	WD_MODE	W/R	Watchdog mode selection. 0: QA watchdog 1: Simple watchdog
[6]	WD_SCALE	W/R	Watchdog clock divider scale. 0: t_{WDCLK_SCALE} = 128us 1: t_{WDCLK_SCALE} = 8192us
[5:0]	WD_CLK	W/R	Watchdog clock divider. t_{WDCLK} = (WD_CLK[5:0] + 1) × t_{WDCLK_SCALE}

CONFIG_WD2 [7:0]			
ADDRESS: 0x0F			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:4]	WD_TCLOSE	W/R	Watchdog close window duration time configuration. Feeding watchdog in close window will trigger a WD_UV violation and increase watchdog error counter by 1. t_{WD_CLOSE} = (WD_TCLOSE[3:0] + 1) × 8 × t_{WDCLK}
[3:0]	WD_TOPEN	W/R	Watchdog open window duration time configuration. Feeding watchdog correctly in open window will restart the whole window cycle immediately. t_{WD_OPEN} = (WD_TOPEN[3:0] + 1) × 8 × t_{WDCLK}

CONFIG_WD3 [7:0]			
ADDRESS: 0x10			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	RESERVED	R	/
[5:4]	WD_FAIL_CNT	W/R	Watchdog error counting times configuration. When watchdog error counter reaches this number, a RESET event will be triggered. 00: 1 time 01: 2 times 10: 3 times 11: 4 times
[3]	WD_EN	W/R	Watchdog enable. 0: Disabled 1: Enabled
[2:0]	WD_1UD	W/R	Watchdog first update extension. This configures the extra length of the first open/close window after entering NORMAL state. $t_{WD\_CLOSE\_1st}$ = (WD_1UD[2:0] + 1) × t_{WD_CLOSE} $t_{WD\_OPEN\_1st}$ = (WD_1UD[2:0] + 1) × t_{WD_OPEN}

WD_KEY [7:0]			
ADDRESS: 0x11			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	WD_KEY	W/R	Watchdog key. The current key can be read from this register and the next key will be updated after the current key written to this register by user. For simple watchdog, writing any value to the WD_KEY register will refresh the watchdog and the value written will be ignored. For QA watchdog, writing the correct value to the WD_KEY register during an open window will result in a window refresh and the WD_KEY register being updated. Writing the incorrect value to the WD_KEY register during an open window will result in a WD_LFSR violation. Writing any value during a closed window will result in a WD_UV violation. LFSR polynomial: x8 + x6 + x5 + x4 + 1

WD_LOCK [7:0]			
ADDRESS: 0x12			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	WD_LOCK	W/R	Watchdog configuration lock protection. AAh: Watchdog configuration registers (CONFIG_WD1/2/3) are writeable. Others: Watchdog configuration registers (CONFIG_WD1/2/3) are read-only.

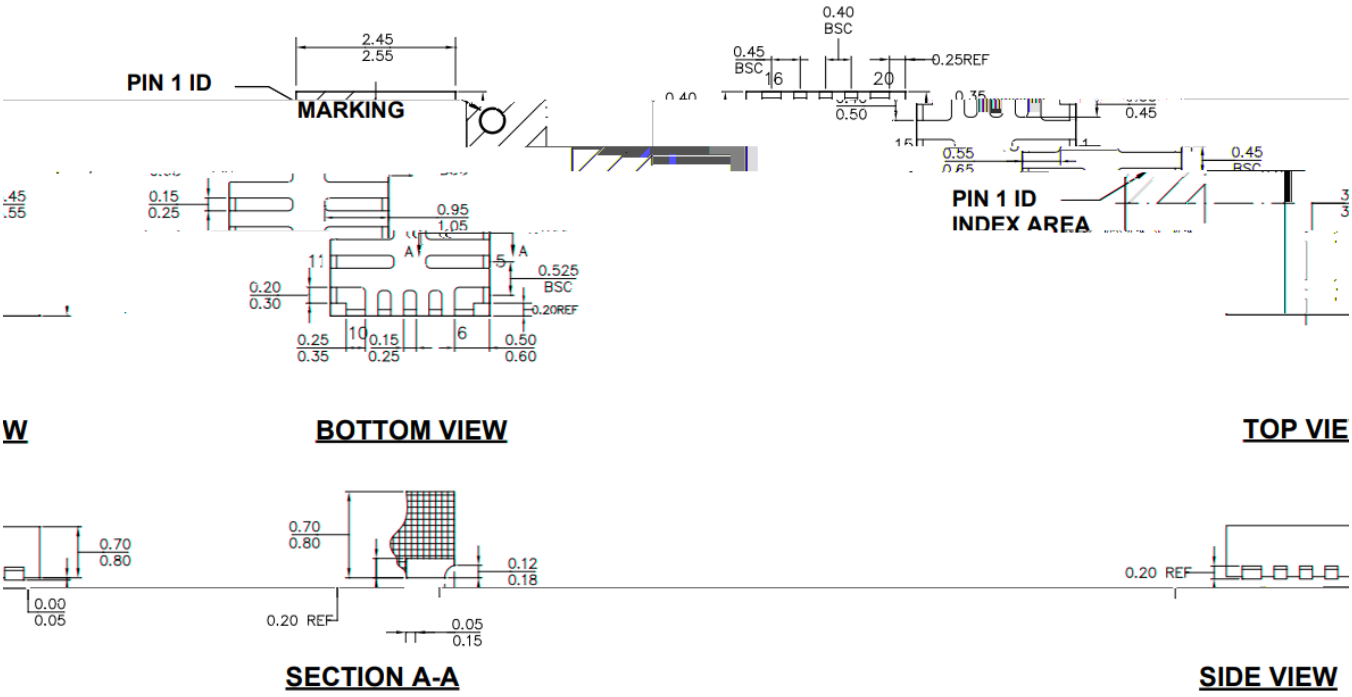
CONFIG_GPIO0 [7:0]			
ADDRESS: 0x13			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	RESETB_DLYR_SCALE	R	RESETB rising delay time scale selection. 0: t_{RST_SCALE} = 0.5ms (0.5~4ms range) 1: t_{RST_SCALE} = 2.5ms (2.5~20ms range)
[6]	RESERVED	R	/
[5:4]	GPIO2_BLANK	R	GPIO2 input signal blanking time after RESETB pulled high. 00: 0ms 01: 2.5ms 10: 5ms 11: 10ms
[3:2]	GPIO2_DLYR	R	GPIO2 input signal rising deglitch time. 00: 80us 01: 40us 10: 20us 11: 10us
[1:0]	GPIO2_DLYF	R	GPIO2 input signal falling deglitch time. 00: 80us 01: 40us 10: 20us 1

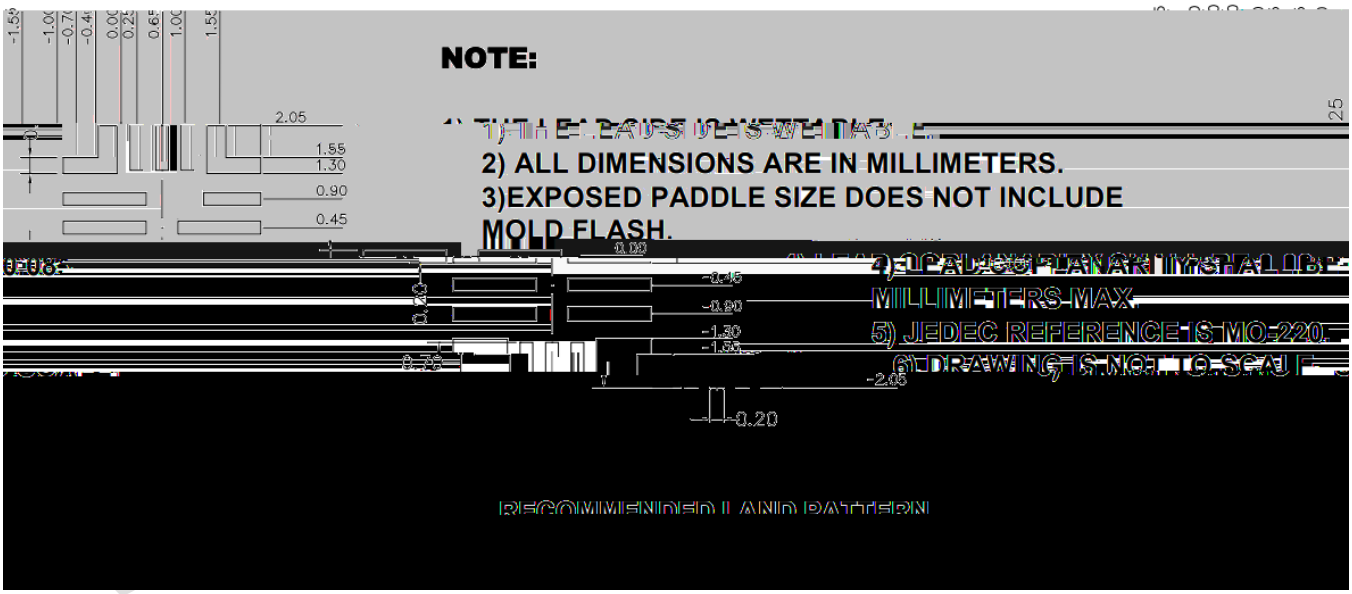
STATUS1 [7:0]			
ADDRESS: 0x18			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	UV5	W1C/R	VMON under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	UV4	W1C/R	LDO4 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5]	UV3	W1C/R	Buck3 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	UV2	W1C/R	Buck2 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	UV1	W1C/R	Buck1 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	OV5	W1C/R	VMON over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	OV4	W1C/R	LDO4 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	OV3	W1C/R	Buck3 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

STATUS4 [7:0]			
ADDRESS: 0x1B			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	RESERVED	R	/
[6]	VCC_OVP	W1C/R	VCC over-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5]	ABIST_ERR	W1C/R	ABIST fault status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	LBIST_ERR	W1C/R	LBIST fault status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	ONLINE_CRC_ERR	W1C/R	Online register CRC fault status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	OTP_CRC_ERR	W1C/R	OTP CRC fault status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	CLK_MON_ERR	W1C/R	Internal clock fault status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	SEQ_ERR	W1C/R	Power sequence fault status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

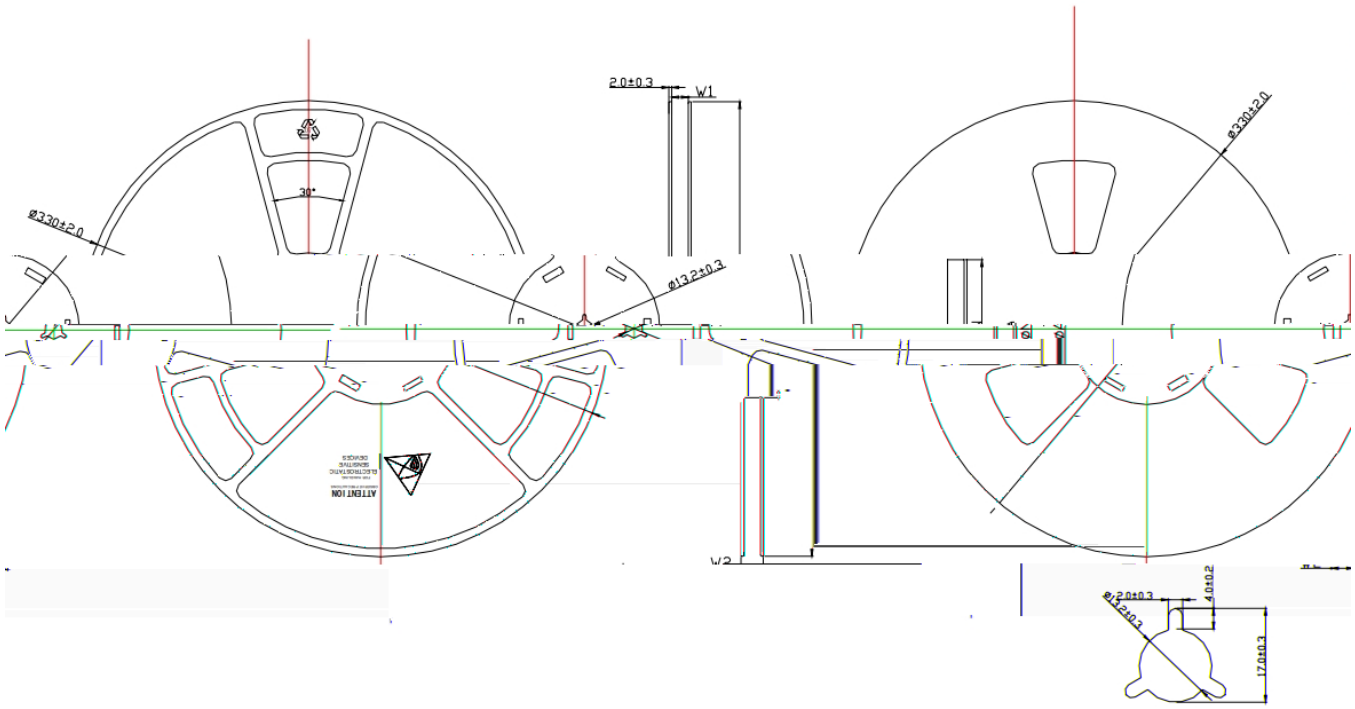
CTRL_ONLINE_ABIST [7:0]			
ADDRESS: 0xE2			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	PASSWORD_ONLINE_ABIST	W/R	Write correct password (D5h) to initiate an online ABIST (Analog Built-in Self Test). After ABIST done, AAh could be read back.

PACKAGE INFORMATION



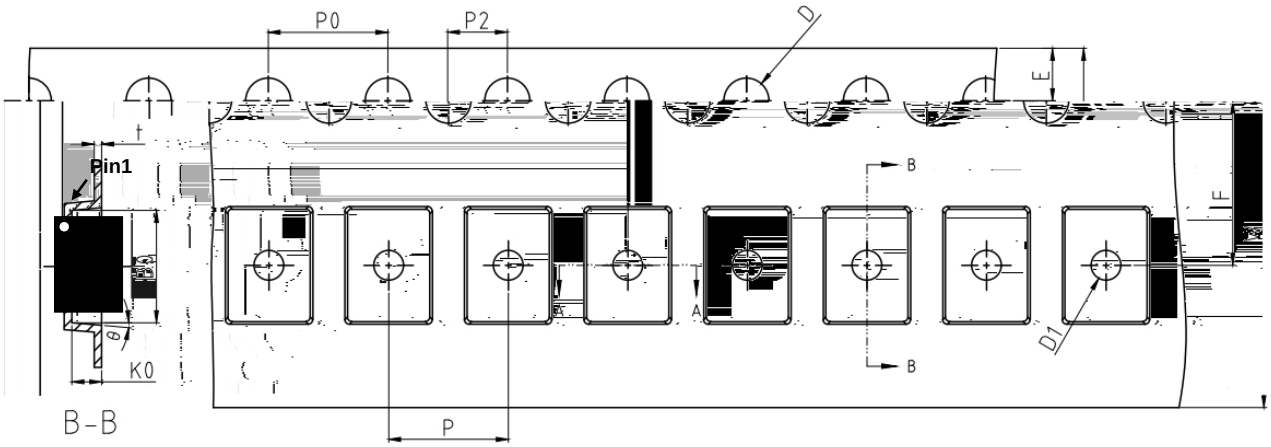


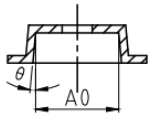
TAPE AND REEL INFORMATION



PRODUCT SPECIFICATIONS

[redacted]





Feed Direction

E	1.75±0.10	W	$12.00^{+0.30}_{-0.10}$
F	5.50±0.05	P	4.00±0.10
D	2.00+0.05		2.75+0.10
Bo	3.75±0.10	D	1.50+0.10
Ko	1.00±0.10	D1	1.00±0.1
t	0.25±0.03	Po	4.00±0.1
θ	5° max	10Po	40.0±0.2

