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Over operating free

		)	)	
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(1)
(2)

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			)))	
			)))	

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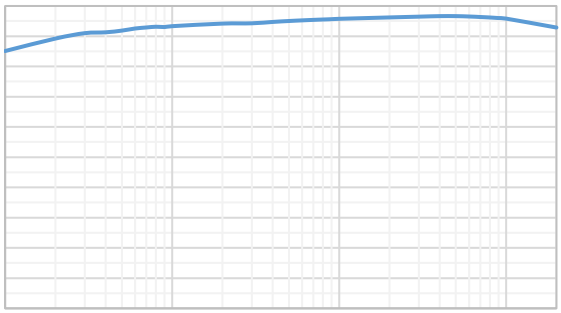

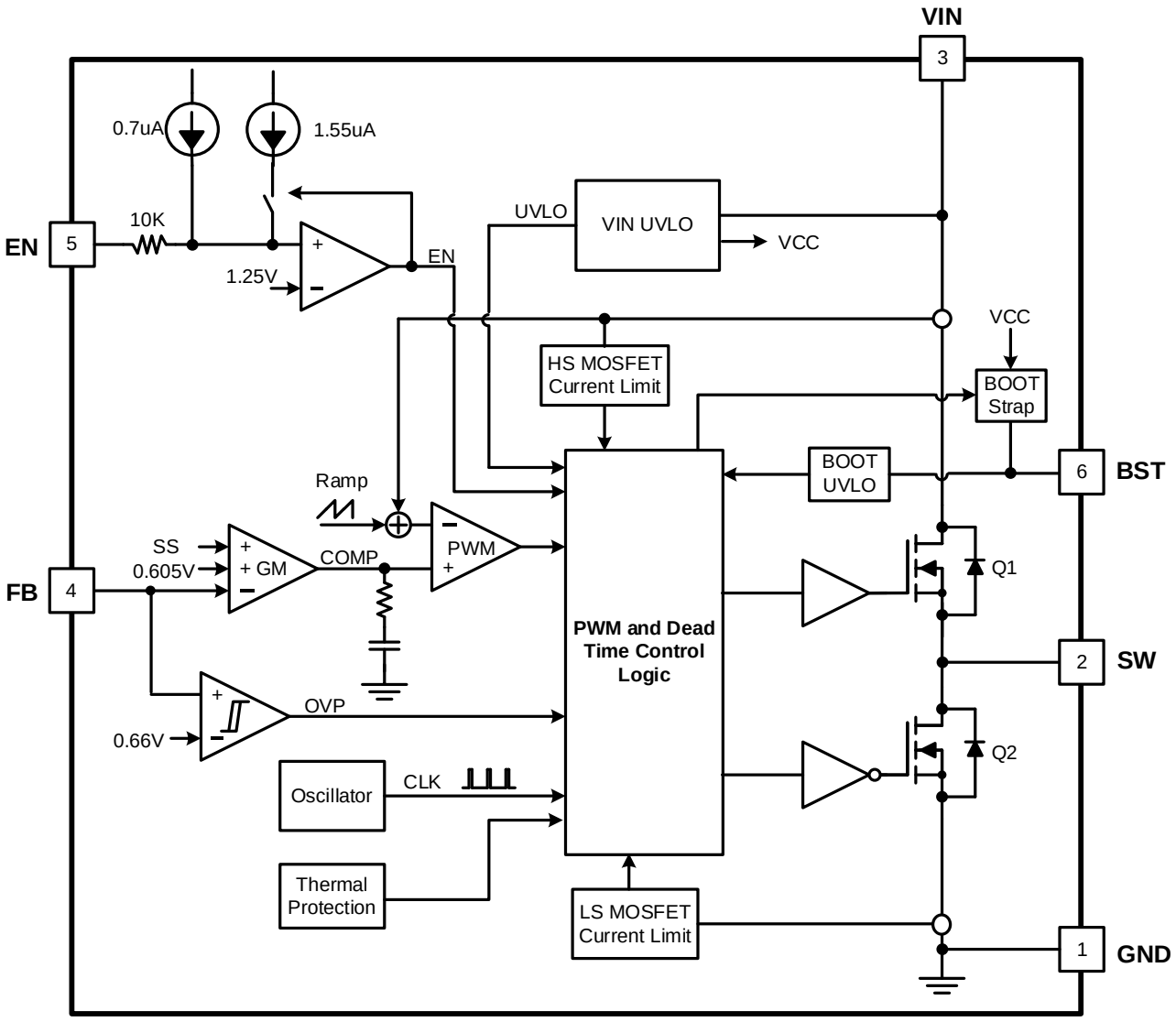
VIN
3
0.7uA
1.55uA
EN
5
10K
1.25V
EN
UVLO
VIN UVLO
VCC
VCC
HS MOSFET
Current Limit
BOOT
Strap
BOOT
UVLO
6
BST
Ramp
SS
0.605V
+ GM
COMP
PWM
FB
4
PWM and Dead
Time Control
Logic
Q1
2
SW
OVP
0.66V
Q2
Oscillator
CLK
Thermal
Protection
LS MOSFET
Current Limit
1
GND

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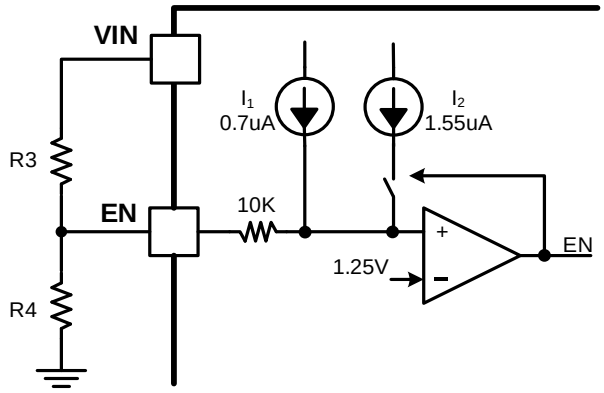

$$MB \quad \frac{NoV\ o \quad \frac{I\ A}{I\ M} \quad No}{D \quad \frac{I\ A}{I\ M} \quad D} \tag{1}$$

$$M \quad \frac{M \quad I\ A}{No \quad I\ A \quad M \quad D \quad D} \tag{2}$$

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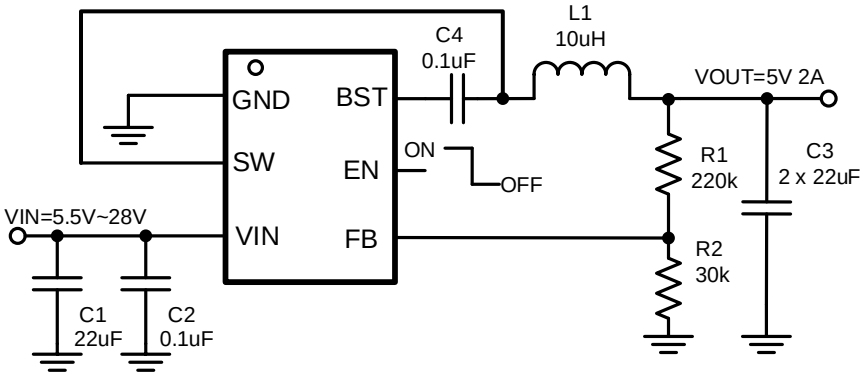


Design Parameters	Example Value
Input Voltage	12V typical, 5.5~28V
Output Voltage	5V
Output Current	2A
Output voltage ripple (peak to peak)	8mV
Switching Frequency	410kHz

)

)

(3)

)

)

)

)

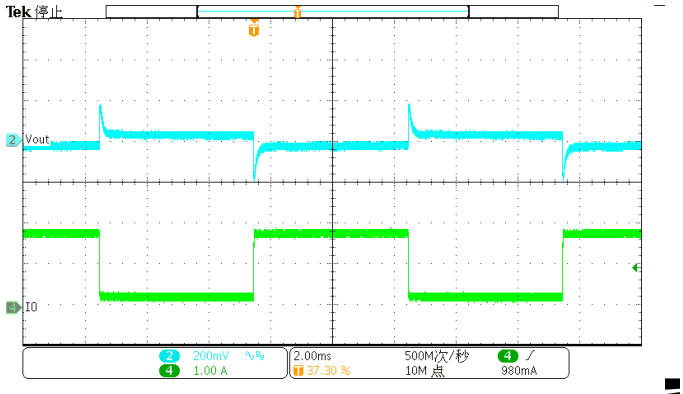
(4)

(5)

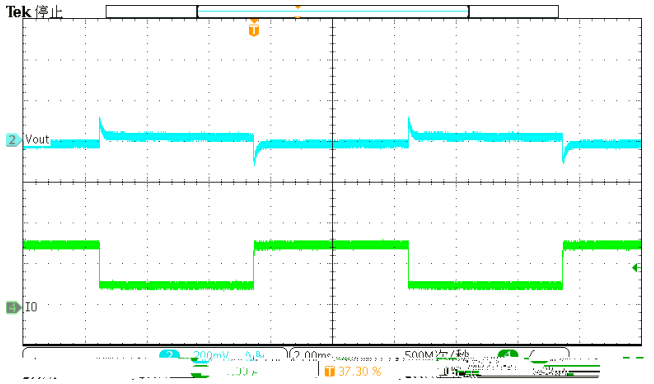
)

)

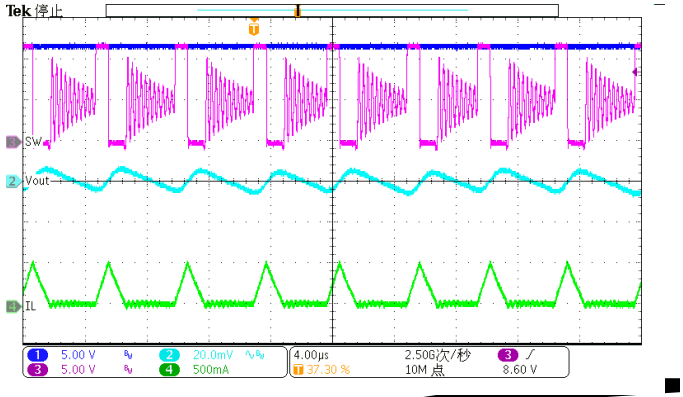
)


Tek 停止
Vout
IO
2 200mV
4 1.00 A
2.00ms
37.30 %
500M次/秒
10M 点
980mA

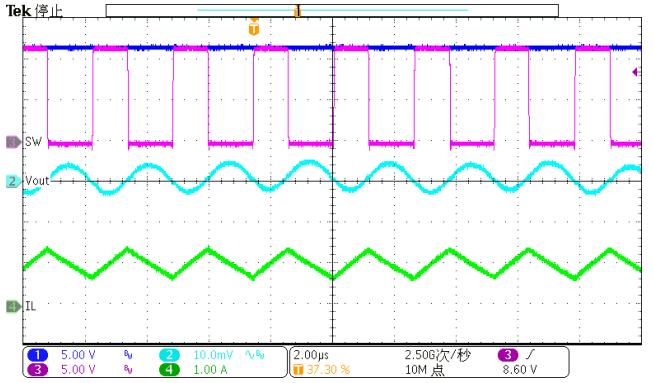
)

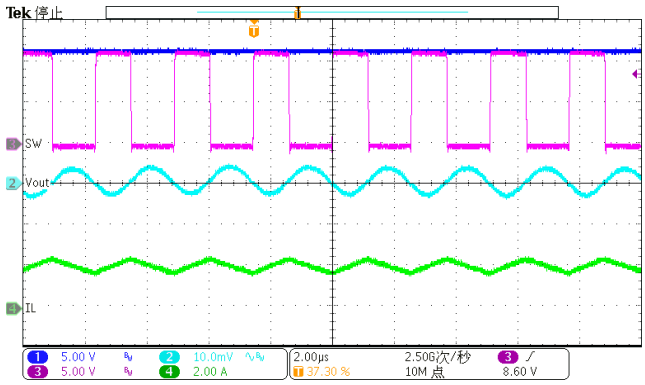

Tek 停止
Vout
IO
37.30 %

)


Tek 停止
SW
Vout
IL
1 5.00 V
3 5.00 V
2 20.0mV
4 500mA
4.00µs
37.30 %
2.50G次/秒
10M 点
3 ∕
8.60 V

)


Tek 停止
SW
Vout
IL
1 5.00 V
3 5.00 V
2 10.0mV
4 1.00 A
2.00µs
37.30 %
2.50G次/秒
10M 点
3 ∕
8.60 V


Tek 停止
SW
Vout
IL
1 5.00 V
3 5.00 V
2 10.0mV
4 2.00 A
2.00µs
37.30 %
2.50G次/秒
10M 点
3 ∕
8.60 V

)

FLUKE
63.9°C
自动 1
67.5
24.4
ε=0.95
BG=25.0
T=100%
8/1/25 04:36:46 PM

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)

)

1.

2.
3.

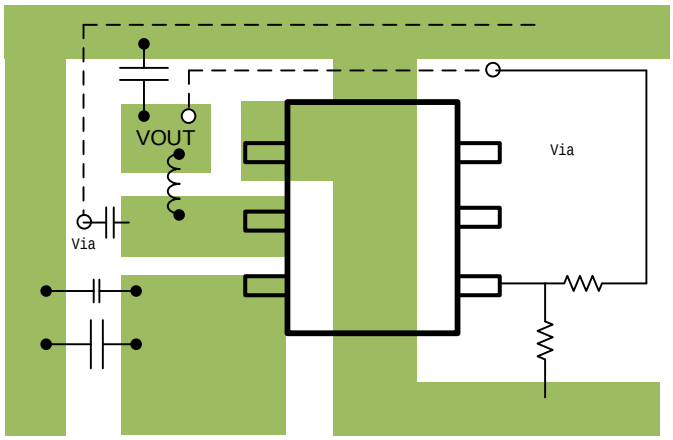
4.
)

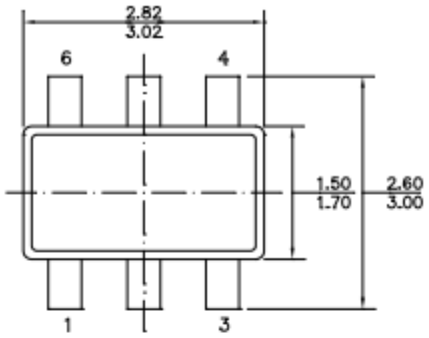
5.

6.

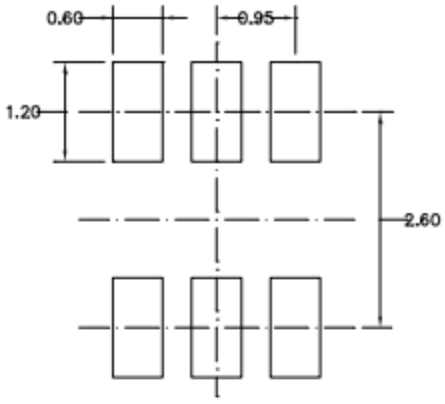
7.

8.

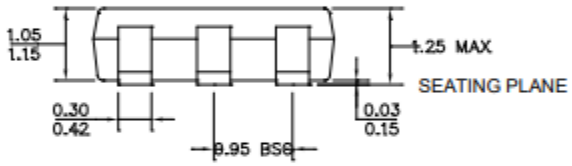


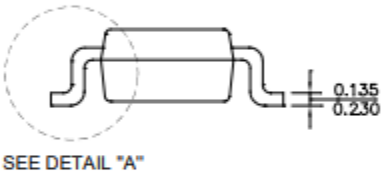


TOP VIEW



RECOMMENDED LAND PATTERN



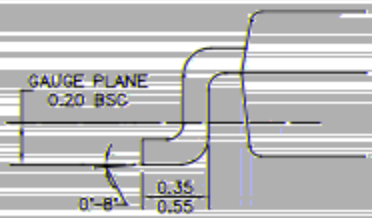


FRONT VIEW **SIDE VIEW**

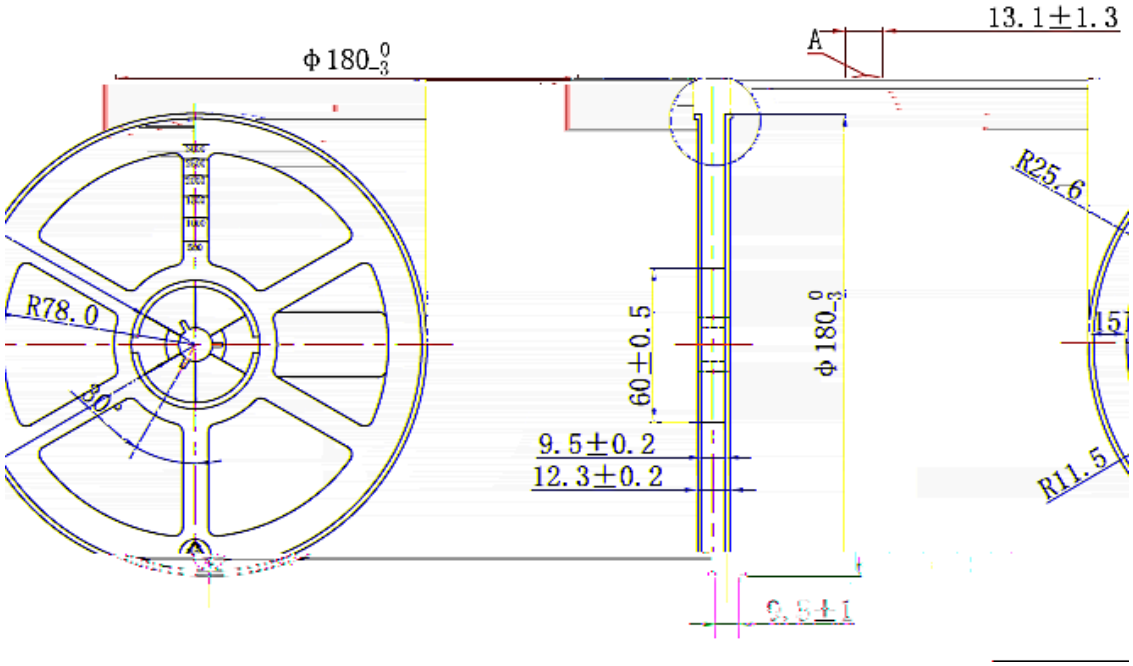
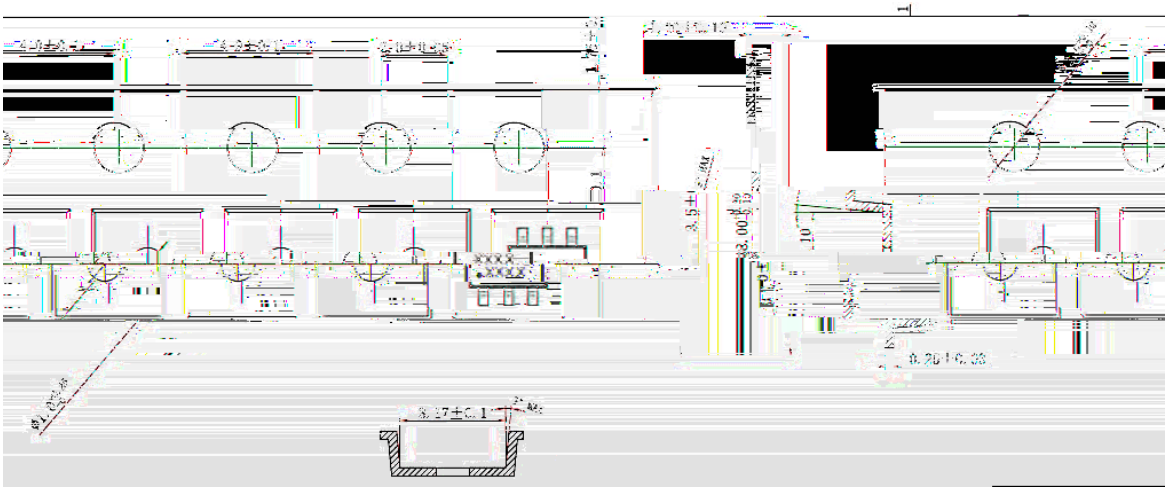
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FL
PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD
OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER
FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIAT
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MA
FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

ASH,
FLASH
ON AB.
RK



DETAIL "A"


13.1±1.3
A
φ180 0 -3
R25.6
R78.0
30°
60±0.5
φ180 0 -3
9.5±0.2
12.3±0.2
R11.5